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Application Note

BE1-810/U Over/Underfrequency Relays: Undervoltage Inhibit Operate Time

The following is a clarification of the operation of the Undervoltage Inhibit function of the BE1-810/U. The explanation is prompted by an undesired trip observed due to mis-coordination of trip and inhibit times. Figure 1, a simplified partial block diagram of the relay, shows the interconnection of the relay elements referred to in this application note. The purpose of the undervoltage inhibit function is to prevent the relay from issuing a trip signal when the frequency measurement should be blocked, such as during generator starting and shutdown or when the voltage source to the relay is interrupted.

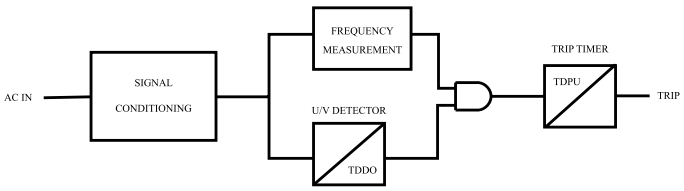

Figure 1 - BE1-810/U Simplified Block Diagram

Operation of Undervoltage Inhibit

The Undervoltage Inhibit function on a BE1-810/U relay does not operate instantaneously. Characteristic of analog circuits, the undervoltage detector dropout time (TDDO in Figure 1) varies with the difference between the Inhibit setting and the actual operating voltage. Figure 2 shows a typical graph of the dropout time versus Inhibit setting for three values of prefault voltages when the voltage is suddenly removed. The graph shows that the dropout time increases as the inhibit setting is lowered, to a maximum of approximately 90 ms for the lowest setting of 40 Volts.

Figure 2 shows that, for a typical factory setting of 80 V and normal operating voltage of 120 V, the operate time is approximately 45 ms.

The potential mis-coordination can occur when relay trip times (TDPU in Figure 1) are set shorter than the necessary undervoltage inhibit time. A low undervoltage inhibit setting, combined with a very fast operate time, can lead to an undesired underfrequency trip. The reported trip was for an application with a 40 Volt inhibit setting and a 4-cycle time delay. Due to the transient response delays of the voltage inhibit circuitry, when both the frequency and voltage decay, a race condition may occur which allows an underfrequency time-out and trip to occur prior to the voltage inhibit circuitry detecting an undervoltage condition.

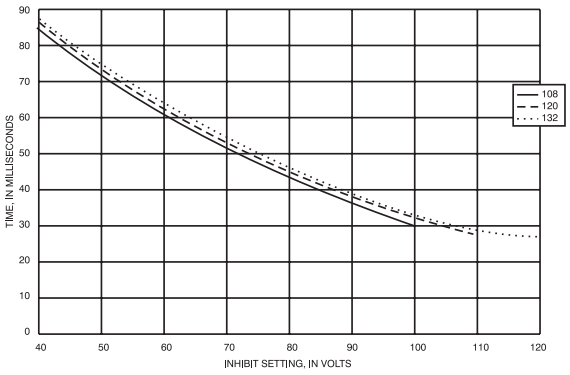

Figure 2 - BE1-810/U Typical Inhibit Timing Characteristic

In consideration of this coordination issue we recommend the settings in Table 1.

U/V Inhibit Setting	Minimum Trip Time (60 Hz)
80 V	3 cycles
40 V	6 cycles

Table 1 - Minimum Inhibit Settings

For More Information

For further assistance with product orders or questions, contact Basler Electric Technical Support at 618-654-2341.

For additional information, including more application notes, product bulletins, and instruction manuals, visit www.basler.com, contact your Application Engineer, or contact Technical Support at 618-654-2341.

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