BUS PROTECTIVE RELAYING, METHODS AND APPLICATION

ABSTRACT

This paper serves as a review of the application of bus protective relaying. Several methods of bus protective relaying are described and compared in the paper, with mainstream emphasis. The methods discussed most in this paper include high impedance unrestrained differential, low to moderate impedance unrestrained differential, low impedance restrained differential, interlocked line and transformer relaying, and overcurrent relaying. Other schemes are only briefly discussed. Current transformer performance, along with the impact of AC and DC offset induced saturation of the transformer, is reviewed. Also, in Appendix A, basic bus design layouts are reviewed.

INTRODUCTION

The operation of a bus protection relay is arguably the most severe operating contingency affecting system stability as well as customer load, at least at critical buses. An understanding of the options for bus protection relaying is, therefore, of value to those working in the protective relaying field.

This paper stresses analysis of those designs using the common magnetic core current transformer (CT). The bus protection methods discussed include:

- High impedance unrestrained differential
- Low to moderate impedance unrestrained differential
- Low to moderate impedance restrained differential
- Interlocked line and transformer relaying
- Overcurrent relaying, including partial differential relaying
- Other less common designs

One should review several good references on bus protection. These include an IEEE standard on bus protection, C37.97 [1], and several texts [2], [3], and [4], and an IEEE standard on application of current transformers, C37.110 [5].

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Since magnetic core CT performance is critical to the setup of these schemes, CT performance characteristics are reviewed first, then each protection method above, as well as several other less common schemes, is discussed and developed in turn. Lastly, some aspects of bus protection dependability (dependable: higher likelihood of operation for in-zone faults) and security (secure: lower likelihood of operation for out of zone faults) are covered.

Note on Resistance and Currents in Examples
For simplification of the examples, all impedances are added algebraically. Also, in most examples, reactances are ignored. This is approximately true (e.g., most CT secondary circuits, as long as the windings are completely distributed and there is no saturation, are mostly resistive). It is a bit conservative in most relay settings, since the computed impedances in this method are higher than the actual impedances. For example, if X=1 and R=1, the net impedance is considered as 2Ω though the actual impedance is 1.41Ω. Using 2Ω results in a higher voltage setting (more secure) for most relay settings, as is clarified later.

CURRENT TRANSFORMER PERFORMANCE CONSIDERATIONS

Critical to the analysis of a bus protection scheme is an understanding of the performance of common magnetic core CTs. For a fault just external to a bus protection zone, the CT nearest the fault will see higher currents than other CTs in the zone though, in radial single source systems, all of the source side CTs also will see the same fault current. Assuming all other CTs are rated the same and have the same ratio, the CT seeing the highest current will usually will be at greatest risk for going into saturation and is usually considered the worst case for which the bus protection system must be designed. There are two approaches to the problem. Either 1) design a system so that CT saturation will not occur, or 2) design a system where the bus protection relay will not operate for the saturation of this CT. The following discussion addresses the mechanisms of CT saturation and how one determines if a CT will go into saturation.

Steady State AC Saturation

The first approach to determine if a CT is rated for its application is to calculate whether the AC voltage that will be impressed on its secondary during a fault will exceed the AC voltage that the CT can support. This typically is done using fundametal frequency values of AC current with no DC offset.

Equivalent Electric Circuit

Most engineers have worked with CT equivalent circuits, with various modifications. The derivation and analysis is available in several of the references [2-5]. One common version is shown in Figure 1.

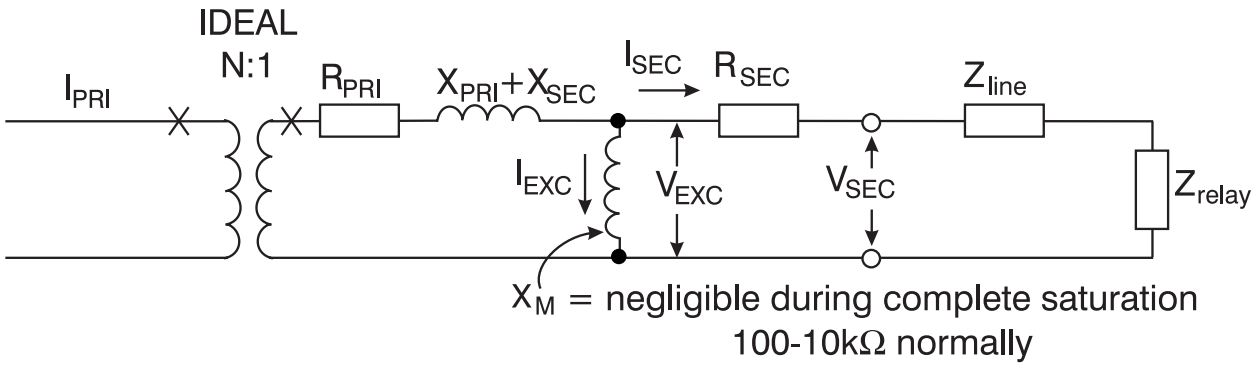

Figure 1: Simplified CT Equivalent Circuit

Note that X_m in the figure is labeled as negligible, or 100-10K ohms. The impedance of the excitation branch varies tremendously from one CT design to the next, the tap ratio used, and the V_{exc} seen by the CT. However, it is the negligible impedance during CT saturation that will most affect relay settings. This low impedance occurs when all of the steel is magnetized at the steel's maximum, yet the primary current flow is oriented toward deeper magnetization. It is not until the primary current wave form reverses direction that the flux level begins to reduce and saturation is removed. The effect may be clearer in the discussions of DC offset effects that follow.

CT, Line, and Relay Impedances

In Figure 1, the CT primary and secondary reactance is shown but is commonly negligible (especially the primary). This reasonably accurate representation is used herein. However, only when a CT has "fully distributed" windings can the CT secondary reactance be considered as negligible without research. Not all CTs have fully distributed windings. Modern CTs are built with fully distributed windings, but it is unclear how long this process has been applied.

Line impedances are typically highly resistive compared to their reactance for the wire size used in CT circuits. In modern low impedance solid state relays, the burden of the relay on the CT circuit is typically negligible.

CT Secondary Voltage Rating

The impedance of the magnetizing branch is non-linear. Its approximate fundamental impedance varies with applied voltage to the CT secondary but typically will be in the several hundred to several thousand ohms range until the saturation voltage level is reached. Note in the CT excitation curve in Figure 2 that, at the indicated ANSI knee point, the magnetizing impedance is about 5000Ω (= 200V/0.04A). The ANSI knee point corresponds approximately to the highest magnetizing impedance of the CT. Above the knee point, small V_{exc} increases cause large I_{exc} increases, which corresponds to a low X_m. Below the knee point, X_m is low, too. For example, at 10V, X_m is about 2500Ω (=10/0.004).

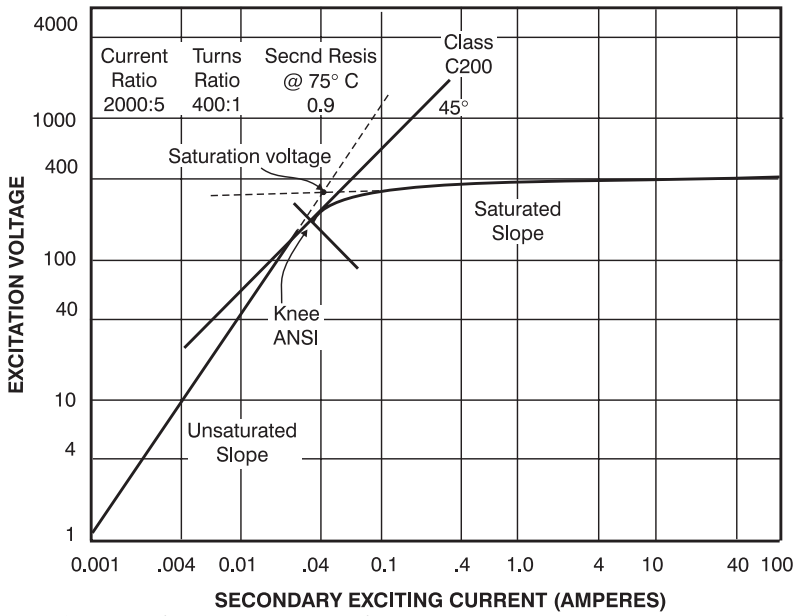

Figure 2: Typical CT Excitation Voltage Versus Excitation Current Curve

The voltage that the CT is rated to drive varies according to one's approach. Three common approaches are:

- The IEEE C57.13 "knee point," constructed using the intersection of the excitation curve and a 45° line as shown in Figure 2.
- The "saturation voltage" using the intersection of straight lines drawn from the two sections of the curve as shown in Figure 2. Some sources refer to the saturation voltage as the IEC knee point. However, other sources definethe IEC knee point as the voltage where a 10% increase in V_{exc} will cause a 50% increase in I_{exc}.
- The "C" rating of the CT (IEEE C57.13-1978, Section 6.4.1.2).

The C rating calls for less than 10% error in secondary current error at 20 times rated current (5*20, or 100A) into 1, 2, 4, or 8W 0.5pf burdens (Note: 0.5pf, I lags $V_{CT,term}$ by 60 degrees), which effectively specifies that the CT shall be able to reproduce 100V, 200V, 400V, or 800V at its terminals with 100A flowing into a 0.5pf burden (60 degree lagging). Besides the corresponding C100, C200, C400, and C800 ratings, there are references to C10, C20, and C50 ratings. The standard is a little unclear in regard to the power factor for the C10, C20, and C50 ratings and can be interpreted to say that either the relaying class 0.5pf specification applies or the metering class 0.9pf specification applies.

Error is based on the concept "(ideal-actual)/actual" using only magnitude measurements. Assume that 110A would be the current out of a perfect CT, but one actually receives 100A. The error is (110-100)/100, giving 10% error. There is an additional error caused by input vs. output phase shift that is not accounted for in relaying class CT accuracy. At voltages below the CT knee point, the excitation current is negligible, so the magnitude and phase angle shift error from a relaying class CT is very small below the knee point. Be aware that

the excitation branch may be actually carrying substantially more current than the missing 10A: The excitation branch, at the saturation point, is carrying substantial harmonic current, and the fundamental excitation current is likely more lagging than burden current. For example, assume the burden on the CT was all resistive, and the excitation branch had an effective fundamental frequency impedance phase angle of 70deg. Assume one had an ideal secondary of 110A@0 deg, and the excitation branch is pulling 29A@70deg. The net output of the CT would be about 100A@-27degrees. An excitation branch pulling 29A would be so heavily saturated that the harmonic content of the output waveform would be huge.

A simplified method to determine the C rating from the curve using a simple algebraic approach, where we assume excitation current is in phase with output current (i.e., the CT burden is mostly reactive, just as the excitation branch is mostly reactive) is as follows:

1) Find V_{exc} where I_{exc} =10.

2) Now calculate the CT terminal voltage with this V_{exc} and 100A secondary, using simple algebraic voltage drop equations ($V_{CT,terminal} = V_{exc} - 100*R_{CT}$).

3) Round down $V_{CT,terminal}$ to the nearest rating, C100, C200, C400, and C800, etc.

As an example, from the above curves:
Rct = 0.9W. At 10A excitation current, the excitation voltage = 300V.
$V_{CT,terminal}$ = 300 - 100(0.9) = 210V, which yields C200 rating.

The sample CT in Figure 2 has an ANSI knee point of about 200V, a saturation voltage of about 275V, and is class C200.

Steady State AC Saturation

The next step is to apply anticipated faults to the system and determine if the voltage that will be impressed upon the CT will be greater than the CT rating:

$$V_{CT,Rated} \geq K \cdot I_{sec,rms} \cdot Z_{sec} \qquad \text{Eq. 1}$$

where Zsec includes the CT internal resistance, and

$V_{CT,Rated}$ = Knee Point, Saturation Voltage, or C Rating, depending on the user's decision
K = User's Safety Margin Factor

The equation must be evaluated for all likely CT secondary current distributions for phase and ground faults.

DC Offset and Residual Flux Induced Saturation

The effect of worst case DC offset, worst case AC current, and worst case residual flux in the CT will almost certainly cause at least a small amount of transient CT saturation in a CT that is otherwise totally acceptable for steady state AC fault current.

Magnetic Flux Level Analysis

The analysis of CT flux levels under the presence of a mix of symmetrical AC and exponentially decaying DC, especially if any modeling of CT saturation is to be included, is a rather involved process. Some sources of information are references previously listed, [1-5], but also [6-10]. Some highlights and simplifications of these works follow.

To provide voltage in a circuit requires a changing flux level in a coil:

$$V = k_1 \frac{d\phi}{dt} \qquad \text{Eq. 2}$$

By integrating the voltage at the terminals over time we can determine the core flux level:

$$\phi(t) = \int_0^t \frac{1}{k_1} V dt + \phi_o \qquad \text{Eq. 3}$$

where

ϕ_o = residual flux level at time 0

Faults develop an AC current with an exponentially decaying DC offset that is expressed by the following equation developed in many engineering texts (e.g. [10] chapter 3):

$$I_{pri}(t) = \left(\frac{\sqrt{2}\, V_{rms,pri}}{\left| R_{pri} + jX_{pri} \right|} \right) \left(\sin(\omega t + \alpha) - \sin(\alpha)\, e^{-tR_p / L_p} \right) \qquad \text{Eq. 4}$$

where

$R_p / L_p = R_{pri} / (X_{pri} / \omega)$

$\omega = 2\pi f$

α = a function of system *X/R* and where in cycle the fault is initiated. Randomly takes the value of any angle.

By assuming that the CT secondary burden is a pure resistance (If it were not, another phase shift component would exist for α and another exponential decay term would arise in the equations [4]-[6].), assuming an infinitely permeable core, and assuming the worst case DC offset by setting $\alpha = -\pi/2$ ($+\pi/2$ would be just as bad), the voltage impressed on the CT secondary will have the form of:

$$V_{sec}(t) = \left(\frac{\sqrt{2}\, V_{rms,pri}}{\left| R_{pri} + jX_{pri} \right|} \right) \left(\frac{R_{CT\,burden}}{CT\,Ratio} \right) \left(\sin(\omega t - \frac{\pi}{2}) + e^{-tR_p / L_p} \right) \qquad \text{Eq. 5}$$

Inserting Eq. 5 into Eq. 3, integrating, and simplifying the equation with a proportionality constant, k_2, yields:

$$\phi(t) = k_2 \left[\left(-\frac{1}{\omega} \cos(\omega t - \frac{\pi}{2}) \right) + \left(\frac{L_p}{R_p} \left(1 - e^{-tR_p / L_p} \right) \right) \right] + \phi_o \qquad \text{Eq. 6}$$

Examination of Eq. 5 shows that k_2 is proportionate to the CT secondary voltage. Hence, the higher either the fault current or burden, the higher the voltage and the higher the flux level. Figure 3 is a graph of the results of the above analysis, showing the flux buildup that will occur in a CT during an event, assuming a pure resistive secondary circuit and an infinitely permeable core.

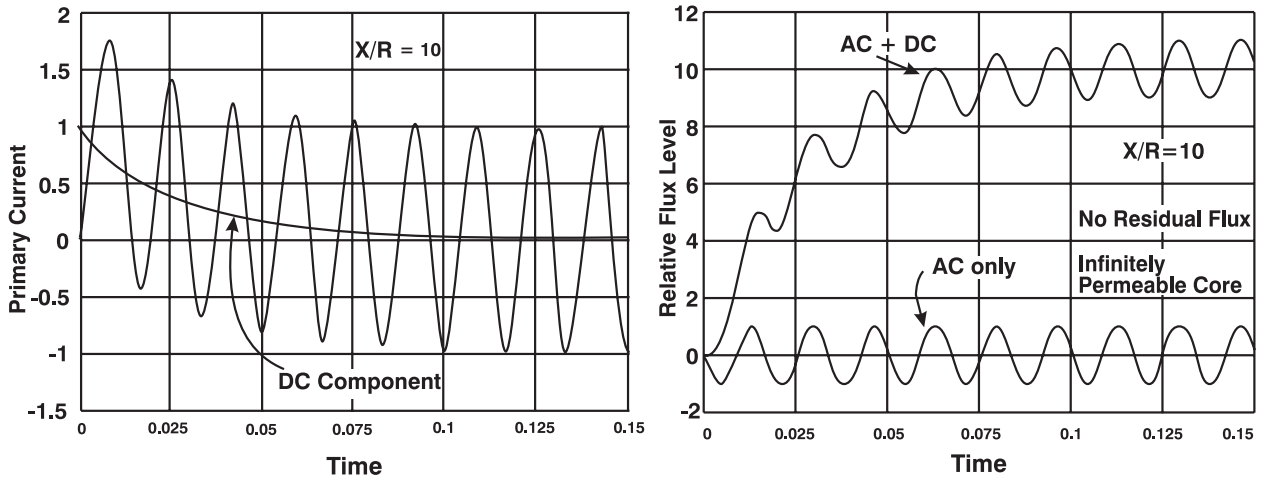

Figure 3: CT Flux Levels with DC Current Effects, Infinitely Permeable Core

Figure 3 does not show any residual flux at the start of the process. All practical magnetic cores hold some level of flux after current is removed, and during normal operation a CT reproduces an AC waveform for an indefinite period with core flux levels that are constantly offset from a zero flux level. The offset tends to be worst immediately after a major reduction in current levels (i.e., after a circuit breaker opens) and tends to decrease with time. High speed reclosing sees larger flux offsets as a result, which tends to cause worse transient CT saturation. In a sample test reported in [5], the residual flux level found in a variety of CTs varied over the range of 0-80% of design flux level. About half of the CTs had residual flux levels above 40% of rated. Residual flux may be oriented in either direction. Hence, the flux indicated in Figure 3 may be shifted up or down depending on the level of residual flux.

Core flux levels, of course, do not reach the levels shown in Figure 3. The core reaches a level of flux density, and flux levels do not appreciably increase after that point. Thereafter, the CT output drops to zero until current flows in the negative direction to desaturate the CT. As the DC offset decays, the CT output gradually improves until the secondary current represents the input waveform. In a real world CT, for the primary current shown in Figure 3, and assuming a maximum relative flux level of 2, the output wave form takes on the form shown in Figure 4. This waveform is for a resistive secondary burden. An inductive burden results in a decayed dropout of the secondary current wave, and the resultant current has more of a sine waveform.

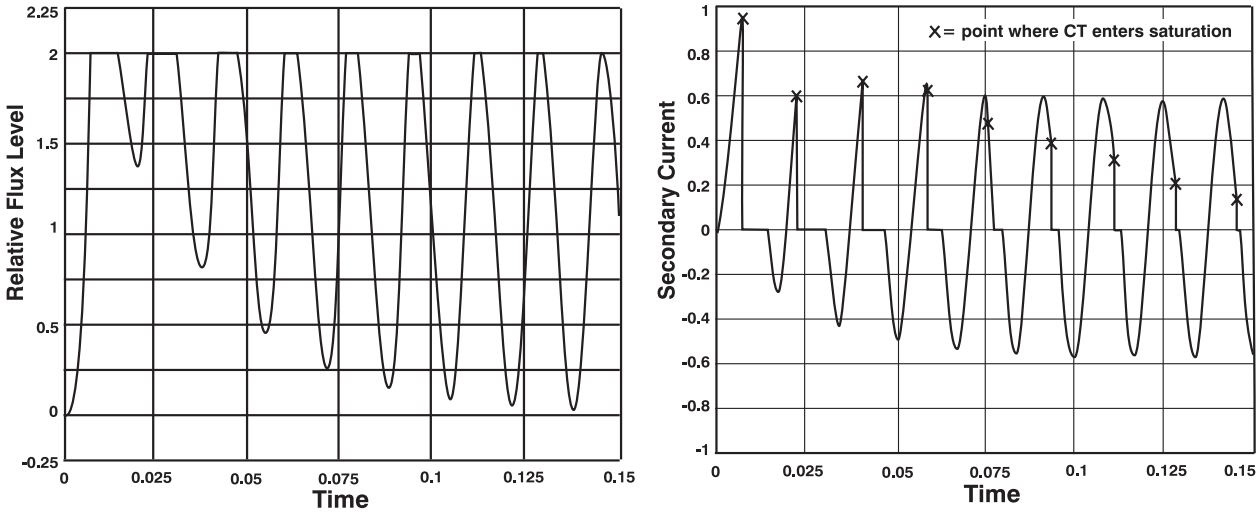

Figure 4: Saturation Effects on a Real World CT

It would be possible to provide “time to saturate” and “time to desaturate” equations, but this is not done herein because exact times are not the point of this exercise and likely a fairly inexact analysis due to unknown circuit impedances, CT magnetic approximations, and pre-event flux levels. (Equations may be found in [5] and [9].) The point is that 1) saturation may occur very quickly, as fast as the first half wave of the primary current wave, and it needs to be accounted for in the setup of a bus differential scheme and 2) given a saturated CT, as the primary current DC offset decays, the output waveform returns to a normal AC waveform. Note that in Figure 4 after about two system time constants (about 0.053 seconds for X/R =10; see eq. 31 for 1 time constant definition), the output wave form has begun to look closer to the normal AC wave form.

Peak Flux Assuming No Saturation

By substituting into Equation 6 for some time well into the future when the exponential DC offset term has essentially been completely integrated, and choosing a point in time where the cosine term comes to 1, we can state the peak flux if there is no CT saturation:

$$\phi_{max} = k_2\left[\left(\frac{1}{\omega}\right)+\left(\frac{L_p}{R_p}\right)\right]+\phi_o \qquad \text{Eq. 7}$$

Comparing the max flux level with and without the *L*/*R* term, noting $x = 2\pi fL = \omega L$, and dropping the initial flux term ϕ_o, we can see a ratio of maximum flux with and without the DC offset:

$$\frac{\phi_{max,dc+ac}}{\phi_{max,ac}} = 1+\frac{X_{L,p}}{R_p} \qquad \text{Eq. 8}$$

Where

$\phi_{max,dc+ac}$ = the peak flux level that would arise from a secondary voltage with both an ac and dc component, and no residual flux effects

$\phi_{max,ac}$ = the peak flux level that would arise from a secondary voltage with only an ac component, and no residual flux effects

A similar equation can be derived where the effects of inductance in the CT secondary is considered. From [5] it takes the form of:

$$\frac{\phi_{max,dc+ac}}{\phi_{max,ac}} = 1 + \left(\frac{X_{L,p}}{R_p} \frac{R_{sec}}{|Z_{sec}|} \right) \qquad \text{Eq. 9}$$

Recall that this X_L/R value refers to the primary circuit. Under fault conditions this typically is on the order of 3-15. This means that to avoid saturation due to DC offset, the CT must have a voltage rating that is 4-16 times the voltage rating required for the steady state AC analysis, ignoring the effects of residual flex levels. When considering the effects of residual flux, the allowance that must be made to avoid all hints of saturation when selecting the CT voltage rating, therefore, may need to be even higher than the 4-16 times ac voltage levels, which few practical designs can meet.

CT Analysis Conclusions

From the discussion above, we can conclude that to avoid all hints of saturation from the effects of DC offset (but ignoring residual flux effects), we need a CT with a voltage rating of:

$$V_{CT,Rated} \geq K \left(1 + \frac{X_{L,p}}{R_p} \right) \cdot I_{sec,rms} \cdot R_{sec} \qquad \text{Eq. 10}$$

where K is some margin/safety factor to account for uncertainties, such as the effects of residual flux and circuit modeling error.

If the effects of residual flux and inductive CT burden are considered, from [5]:

$$V_{CT,Rated} \geq \frac{K \left(1 + \left(\frac{X_{L,p}}{R_p} \frac{R_{sec}}{|Z_{sec}|} \right) \right) \cdot I_{sec,rms} \cdot |Z_{sec}|}{1 - (\text{assumed residual flux, in per unit})} \qquad \text{Eq. 11}$$

Assumption of CT Saturation For External Faults

The effect of the two equations above is that for a CT to be completely immune to DC offset it must have a voltage rating that is many times what it needs for the same waveform without the DC offset. This is a difficult demand to make of most installations, and, therefore, in many applications saturation is an assumed possibility. For high impedance bus differential relaying the assumption of possible saturation becomes even more of a necessity because of the speed of the relay and the sensitivity of this type of relaying to CT error.

The process of calculating settings to prevent operation for the saturation of one CT for an external fault is described in forthcoming sections of the paper.

CT Saturation: Is it really a big concern?

It may be asked, “If CT saturation is such a concern for this application, why does it not seem to be a problem with all of my other relaying schemes?” There are several answers.

1) For a bus differential scheme, the saturation tends to cause misoperation, but for line relaying and overcurrent relaying the tendency is toward delayed tripping. The amount of delay involved is not commonly a problem with line relays, but the misoperation of a bus differential relay is likely a major problem.
2) Some high speed line relays make their tripping decisions within a cycle, before the effects of DC offset saturation come into full effect in some cases.
3) The effects of DC offset die out after a period. The effects of DC offset are short. Typical system X/R ratios are in the range of 3-15, yielding L/R time constants of 0.5-2.5 cycles on a 60hz base. After the DC offset passes, the CT starts to put out better current waveforms, allowing the relays to make correct decisions again. The worst window of CT error is likely less than 10 cycles in duration.
4) Saturation is rarely complete, and even a saturated CT puts out some current and voltage.
5) There is a probability factor. a) The DC offset factor in Equation 4 is reduced as α moves from $\pm\pi/2$, b) the initial residual flux may actually be oriented toward reduced likelihood of saturation, and c) Even if the initial flux is oriented toward saturation, data in [5] indicates that only perhaps 50% of the time it is greater than 0.4 per unit.

HIGH IMPEDANCE BUS DIFFERENTIAL RELAYING

Basic Concept

High impedance bus differential relaying is the leading means of bus protection on high voltage buses and critical medium voltage buses. It also becomes more predominant on high fault duty switchgear where the enclosed space of the bus allows little room for dissipation of arc energy.

The basic concept is, of course, that current into a bus must equal current out, and if it does not, the difference current flows through a high impedance operate circuit, raising voltage at the summing point. If there are minor imbalances in the CT currents, the excitation branches of the CTs, and to an extent the relay, absorb the error. But, based upon relay voltage and current settings, there is a point where the voltage is considered too high and a trip ensues. In some designs, current flow in the relay is also monitored and is part of the tripping process. There are two approaches on design of the voltage and current element interaction in the tripping process, both of which are described below.

Relay Operation Analysis

An AC connection diagram of a high impedance bus differential system is shown in Figure 5. In large substation yards the summation point for the CTs is frequently made in one or more sub-panels in the yard.

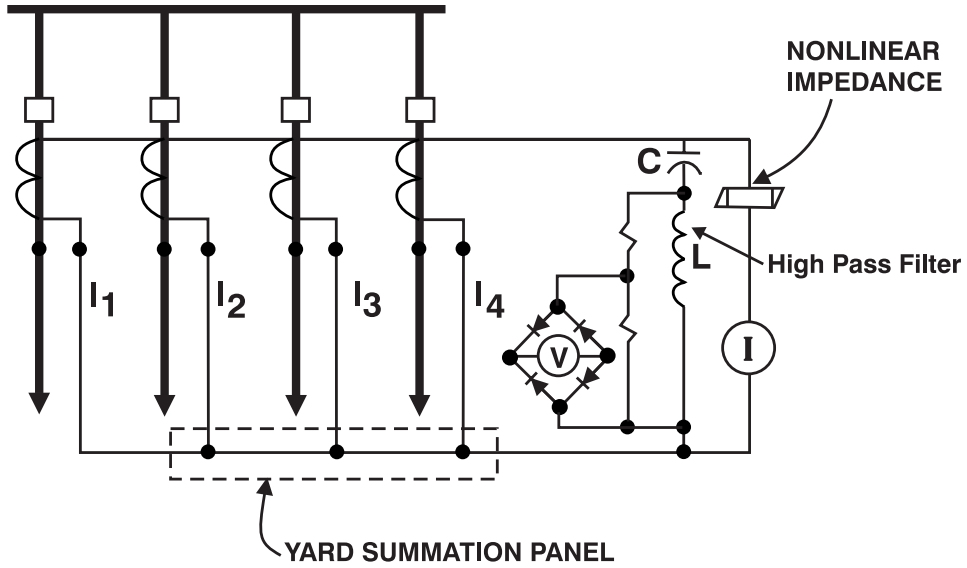

Figure 5: AC Connection Diagram, High Z Bus Differential, Non-Linear Impedance Design [13]

CT Ratios

For CT currents to balance, all CTs must have the same turns ratio. This need for all CTs to have the same ratio can be a major difficulty of this type of bus protection. In distribution substations some compromise of using CT thermal rating factors (1.33, 1.5, 2, 3 or 4) on the incoming breaker and using a high CTR the CTs on the feeder breakers is required.

There are means of making the 87B relay work with CTs that have different ratios [5], [11] and material to follow. This is not an ideal arrangement and should be avoided if possible. The means that might be considered include 1) using partial taps on multi-ratio CTs, possibly using auxiliary CTs, 2) interconnecting CTs in an auto-transformer arrangement, or 3) connecting CTs in a parallel arrangement. These techniques will be covered more fully later in this paper.

Operation During Non-Faulted and External Fault Conditions

The relay should monitor the error current in the CT summation point. For a four input CT summation, for any given phase A, B, or C the summation is:

$$I_{error} = \frac{I_1 + I_2 + I_3 + I_4}{CT\ Ratio} = 0, ideally \qquad \text{Eq. 12}$$

This error current has two paths to follow: 1) through the relay voltage sensing element, 2) through the relay non-linear impedance, or 3) through the CT excitation branches.

Hence:

$$I_{error} = I_{relay,voltage\,element} + I_{relay,non-linear\,impedance} + \sum_{ct1}^{ct\,N} I_{excitation} \qquad \text{Eq. 13}$$

This equation will be used further in this paper to analyze the sensitivity of the relay to internal faults. Until that point, it may be helpful to understand the significance of the equation by analyzing what occurs if an error current is artificially injected into the summation point. In actual practice, this is done as one means of checking bus differential CTs for short circuits. In the typical bus application, under normal operating conditions the voltage measured at the relay, measured between phase and neutral, is less than one volt, sometimes less than one tenth of a volt. It is difficult to tell a normal operating condition from a condition where a CT has inadvertently been left with a short on it after a maintenance period. The practice is to apply a voltage or inject current at the CT summation point and see what current or voltage results.

Let us assume that 0.06A is injected into the CT string by a test device. What is the voltage at the relay?

The relay voltage unit presents about 1000-10,000Ω to the CT circuit at normal operating voltages, depending on the manufacturer's design and relay settings. The non-linear impedance current draw must be taken from graphs supplied by the manufacturer. The CT excitation curve also must be derived from graphs. Hence, finding the steady state summing point voltage for a given error current becomes an iterative process of assuming a voltage at the CT summation point, examining the curves and graphs, summing currents, until a solution is determined. Having done this for one relay design, it was found that, for an injection of 0.06A:

$$\begin{aligned} I_{voltage\,element\,@1700\Omega} &\approx 0.018\,A \\ I_{non-linear\,impedance} &\approx 0.002\,A \\ I_{CT\,1,2,3,4} &\approx 0.01A_{each} = 0.04\,A_{total} \\ V_{summation\ point} &\approx 30V \end{aligned}$$

So, if we inject 0.06A, we should sense roughly 30V at the CT summation point, or conversely, if we apply 30V, we should sense the flow of 0.06A. If 0.06A does not cause about 30V, there is an indication of CT or wiring problems.

Operation for External Faults

There are two settings to be made on the relay: the voltage pickup setting and the current pickup setting, selected to prevent operation for external faults.

Relay Voltage

As discussed at the end of the CT analysis section above, the worst case condition for which the relay must not operate is the complete saturation of a CT during an external fault (typically the CT nearest the fault). The relay voltage setting is based on this condition.

Since each manufacturer has different calibration and safety margins built into its design, the following settings discussion attempts to remain somewhat generic.
In general, the process begins by assuming that an external fault occurs and the current is flowing at maximum bus fault levels toward the fault. Next, one assumes complete saturation of the CT nearest the fault. When the CT saturates, it is assumed that no other CT saturates. The CT saturation is assumed total, as if the core can accept no additional flux. Hence, the CT acts as a negligible reactance air core reactor. Thus, the CT impedance is reduced to the secondary winding resistance in series with the line resistance. The relay voltage setting is chosen to ensure that the voltage developed across the relay under this condition will not exceed the tripping voltage of the relay.

At each CT, the maximum fault level just outside the zone of protection, adjacent to each CT, is calculated. Using the fault current and CT ratio, the current that flows in the CT leads is calculated as if the CT had not saturated. However, the current is considered driven into the saturated CT by other good-performing CTs rather than by the CT's own internal current transformation effect. This causes a voltage rise at the CT summation point, conceptually shown in Figure 6.

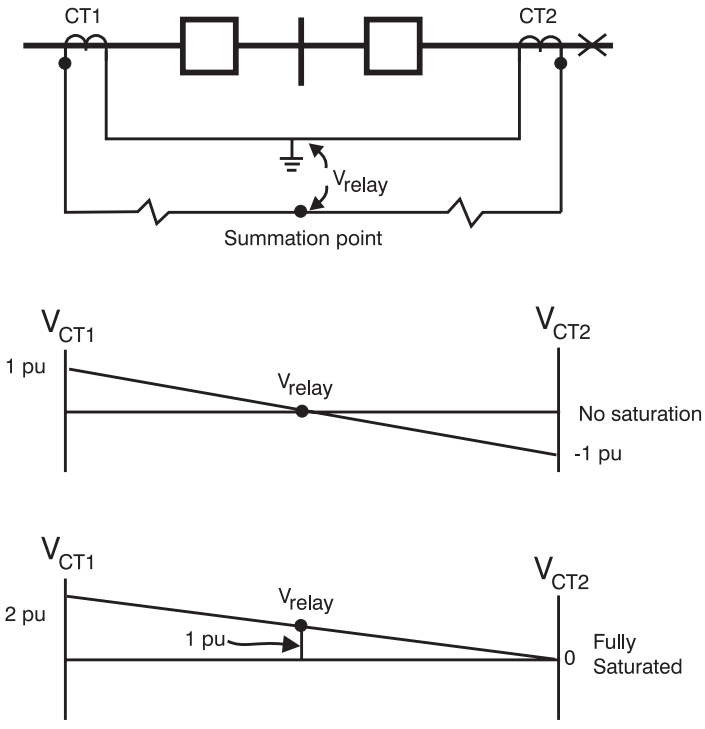

Figure 6: Concept Voltage Profile, Non-saturated and Saturated CT

The voltage impressed upon the relay connected across the summation point can be calculated using anticipated current and lead impedance. This must be evaluated for both phase and ground faults, noting the differing primary currents, lead lengths, and neutral wire currents in each case, taking into account that current may not return all the way back to the control house if yard summation cabinets are used. This must be evaluated for a

fault on any line. The worst case is typically associated with a phase-to-ground fault on the weakest in-feed line. Equations used are:

$$V_{max\,sc,sum\ point,3\,ph} = \frac{I_{max\,sc,3\,phase}}{CTR}(R_{wires\,to\,sum\,point} + R_{CT\,internal}) \qquad \text{Eq. 14}$$

$$V_{max\,sc,sum\,point,ph-gnd} = \frac{I_{max\,sc,phase-ground}}{CTR}(2 \cdot R_{wires\,to\,sum\,point} + R_{CT\,internal}) \qquad \text{Eq. 15}$$

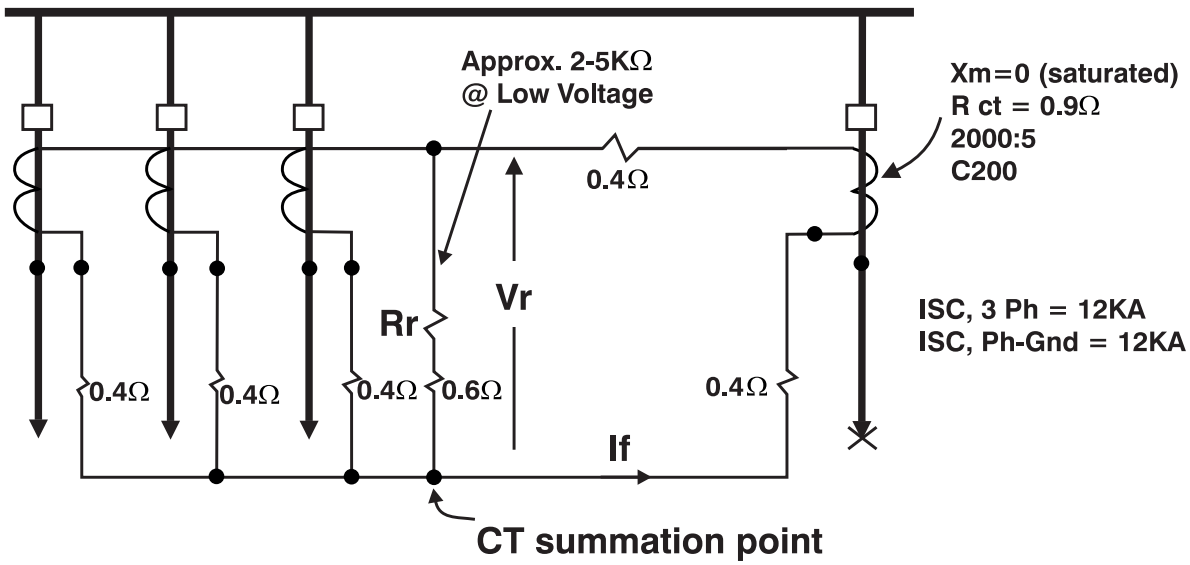

Figure 7: Example CT Secondary Circuit with 1 CT Saturated for an External Fault

The I_{sc} currents used in the calculation above are the RMS fundamental values. They do not include accommodations for DC offset because the relay is either 1) tuned to respond only to the fundamental frequency component of the applied waveform, rejecting DC offset effects, or 2) calibrated to peak instantaneous values associated with a DC offset AC waveform.

Using the data in Figure 7, the voltage (V_r) found for a single line-to-ground fault on a feeder with no contribution to the bus fault duty is:

$$V_{max\,sc,sum\,point} = \frac{12{,}000}{2000{:}5}(0.4 + 0.4 + 0.9) = 51V$$

The voltage unit is set at a level corresponding to the voltage calculated above, but offset from this voltage by some margin factor guidelines given by the manufacturers. The assumption of total saturation also includes a safety factor because in actual practice total saturation likely does not occur.

Ideally, the voltage set point would be no higher than the $V_{knee\ point}$ of the CT excitation curve but this is not critical, and manufacturers have guidelines by which the relay will work

successfully with settings above the CT knee points. However, for secure and reliable performance during an internal fault:

$$K(V_{Highest}) \leq V_{relay} \leq V_{ct,rated} \qquad \text{Eq. 16}$$

where

$V_{Highest}$ is the highest summing point voltage calculated for an external fault during the saturation of one CT, as previously described
K refers to the manufacturer's setting margin guidelines
V_{relay} refers to the relay voltage setting
$V_{ct,rated}$ refers the CT voltage rating, e.g., the ANSI knee point voltage

From the example CT, using the earlier V_{max}=51V calculation, and assuming a margin of 2, one might set the relay to operate at 100V.

Manufacturers' calibration point of the pickup setting varies. In the static switch-based relay design, described later, the voltage pickup of the relay when symmetrical AC voltage is applied is twice the voltage setting [12] [14] (e.g., for a 100Vac pickup setting, 200Vac must be applied to cause a trip). The relay design expects that during internal faults, when the relay is basically presenting an open circuit to the CTs, that the CT will produce the high multiples of knee point voltage previously mentioned and during an external fault the relay must not operate for a fully offset current waveform.

Will the Assumed CT Saturation Really Occur?
The voltage setting began by assuming the CT nearest the fault would saturate. Could this really occur? Comparing the previously calculated 51V for an external fault to the CT rating of about 200V, it is apparent that the system is not at risk of going into saturation for an external fault if we ignore the effects of DC offset and residual flux. But assuming a system X/R ratio of 10, and applying equation 10, and no safety margin or account for residual flux, yields a voltage requirement of:

$$V_{peak,ideal} = 51 \cdot (1+10) = 561V$$

Since the CT is rated at about 200V, it appears at risk to enter into saturation due to DC offset effects.

Relay Current

In the non-linear impedance-based relay design described below, the overcurrent element and voltage element trip contacts are in parallel. The overcurrent element monitors the current through the non-linear impedance. In this design, the setting is intended to add dependability. A typical current setting is equivalent to the current passing through the non-linear impedance when the voltage at the relay is equal to the relay's voltage setting. Consult the manufacturers' manuals for more information.

In the static switch design, the relay output is supervised by the overcurrent trip element. The tripping process is: first, voltage is seen, then the static switches are turned on, then current flows in the relay, and then the relay trips. The overcurrent element is, therefore, set for security and is set to block operation for unrealistically low current faults that may be indicative of a false operation of the voltage element.

One situation in which current pickup may be used to add security is for faults on the secondary of a station service transformer on a bus but not included in the bus differential CT circuit. Such a fault will tend to make a bus differential relay operate in some circumstances. The static switches will quickly turn off on the next cycle if the voltage detected was transient in nature. For example, assume a 13.8kV, 150kVA station service transformer with a 3% impedance is not included in the bus differential scheme. Normal full load current of about 6.3 A is not enough differential current to be sensed by the relay. However, a fault on the secondary of the transformer will produce up to 210A primary. This is likely enough to cause the CT summation point voltage to rise high enough to cause the relay voltage element to operate, but only about 0.52A secondary current on a differential scheme using 2000:5 CTs. The relay can be set to block operation for current below 1A and allow the transformer secondary overcurrent protection to operate. The overvoltage alarm output on the relay could be set to trip via a backup system after some time delay if the transformer protection failed to clear the fault. By setting the current pickup at possibly 5A, a fault in the lower part of VT and station service transformer windings may be withstood without a differential operation.

Operation for Internal Faults

During an internal fault, the CTs attempt to drive current into the high impedance relay. Describing what will occur is dependent on some familiarity with the relay design, but a description of relay design is a few pages forward in this paper. If one is not familiar with how a high impedance differential relay works, one may need to return to this material.

Recall the earlier discussion about CTs where in equation 3 it was pointed out that flux is an integration of voltage. When an internal fault tries to drive current into the high impedance of the relay, the CT voltage rises extremely fast and reaches a tripping voltage in an extremely short amount of time. The area under the voltage vs. time curve, at least to the time when tripping voltage is reached, is extremely small because the time is so short. Since the area under of voltage vs. time curve is small, the net integration of V is small, so the net flux in the CT has increased only slightly before a trip occurs. Hence, the CT does not have a chance to saturate before the trip occurs.

The concept is shown in figure 8. In this graph, current is assumed to be sinusoidal with no DC offset, and we are looking at a half cycle of current. At the outset of the fault, the voltage rises extremely fast. The scale of the drawing does not allow for showing how fast voltage rises. To see how fast voltage rises and then is clamped, let us first look at an SCR based relay (a relay that clamps voltages with SCRs). In the typical bus application, there may be around 50A (10 times nominal current) at the CT secondary trying to flow into the

relay. If we look solely at the 60Hz input impedance of the relay (for example, the Basler BE1-87B had an input impedance of about 5000 Ω, which is somewhat capacitive), we might imply that an extremely steep voltage wavefront would be generated. To actually analyze this condition, the R, L, and C components of all CTs, CT leads, and the excitation impedance of all CTCs need to be analyzed in an EMTP/ATP type program. The effective transient impedance is beyond the scope of the author's ability to estimate well, but let us assume the net parallel impedance of the CT circuit and the relay, as seen at the relay terminals, can be modeled as 500 ohms at 60Hz. This implies that a peak voltage of nearly 35kV is feasible (VPeak=Sqrt(2)*50*500) within 1/4 cycle. This implies an average Volts/second change of around 8.4e6 volts/second (35 kV is reached in 1/4 of 1/60 s, or 35kV*60*4). One can deduct that the tripping voltage is reached quite quickly.

Before proceeding, it may be noted that in an SCR based relay, the SCR's firing decision is based on instantaneous voltage, and the voltage is almost completely unfiltered. In the Basler BE1-87B, the relay is designed so that the SCRs turn on at $V_{SCR,Fire}$=Sqrt(2)*2*V_{set}. The "2" factor is used to account for worst case DC offset in the current waveform. If one sets the relay to trip at, for instance, 100V, and tests the relay to find at what DC voltage the relay will trip, it will trip at 283V. An SCR takes a few microseconds to turn on, and counting other delay factors in relay electronics, the relay may take on the order of 7 microseconds to fully turn on the SCRs. If the voltage is rising at 8.4 million volts/second and the SCR takes 7 microseconds to turn on, then the peak voltage is 283+(8.4e6*7e-6) or about 340V. When the SCRs fire, the input impedance of the relay is brought to very small levels, and the voltage across the relay is reduced to very low levels (much less than 10V, maybe as low as a 1-2V) which further reduces the tendency of the CT to enter saturation. The Basler BE1-87B, at its highest voltage setting (400V, which corresponds to a 1130Vdc trip level), will tend to clamp voltage at around 1500V peak, as described at the start of this paragraph.

For a non-linear impedance based relay (i.e., one that uses some version of a surge arrester), after the surge arrester begins to conduct, it does not drive the voltage down as low, but limits further rise in voltage. Hence, the voltage at the CT remains high for a longer period. High voltage and high current are the elements of heat, so there will be much more heat generated in the non-linear impedance compared to the SCR. Hence, the non-linear impedance is more subject to heat damage, and there will be much more tendency for the CT to enter into a transient saturation on each positive and negative swing of the current cycle. The risk of heat damage increases the need for fast clearing of the fault or shorting of the CTs by a lockout relay contact.

One does not really need to be concerned much with the details of the maximum surge voltage that the high impedance bus protection relay will see and the possibility of damage. The huge installed base of both the SCR and non-linear impedance type relays and their successful implementation over many years, indicates that the systems have been properly designed for the peak voltages that can be found in the CT circuit system during an internal fault.

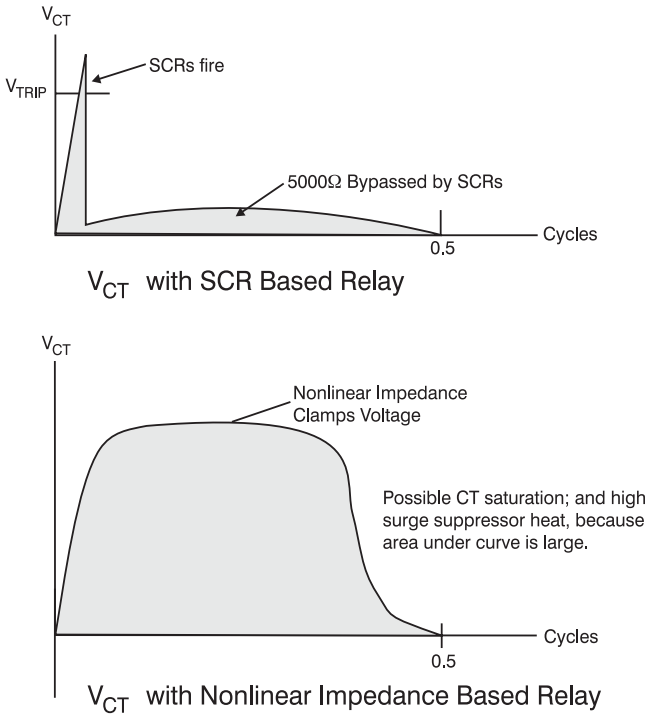

Figure 8: VCT During an Internal Fault

The sensitivity of the relay to internal faults is determined by the CT ratio, CT excitation currents, and the current the relay will pull at trip level currents. The process is to find the excitation current that will flow in all parallel CTs at the set point voltage, add the current in the relay, then multiply by the CTR.

$$I_{fault,min} = CTR\left(I_{relay,voltage\,element} + I_{relay,non-linear\,imp.} + \sum_{ct\,1}^{ct\,N} I_{exc.} \right) \text{ calculated at trip voltage} \quad \text{Eq. 17}$$

Typical applications yield sensitivities in the 30-200A range. For example, using the previous CT excitation curve, a relay setting of 100V, 4 CTs in parallel and one manufacturer's relay [13]:

$$I_{fault,min} \approx 400\left(\frac{100}{1700} + 0.01 + 4 \cdot 0.022\right) = 400 \cdot 0.157 = 63\text{A}$$

Recall that the SCR-based relay is designed to trip at 2 times its setting when steady sinusoidal voltage is applied, which affects the voltage used in eq. 17, and may involve estimations of CT performance as CTs reach saturation..

Mixing Different Ratio CTs

On occasion, different ratio CTs need to be mixed in a high impedance bus protection scheme. The common cause is placement of a new breaker in a substation that has a much different (usually higher) steady state current rating than existing older breakers. The CT ratios cannot be matched. Three methods that could be used to work with the mixed CT ratios were briefly mentioned earlier (page 11, under "CT Ratios").

1) Use Partial Taps on CTs

The approach of using partial taps on multi-ratio CTs has two difficulties: CT overload and high voltage across the open terminals. Suppose one faces a case of mixing 3000A and 1200A breakers on the same bus. As may be typical, assume that the 1200A breaker has only 1200:5MR CTs, so the approach one must consider is tapping the 3000:5 CT at 1200:5. The first concern is immediately seen: If 3000A flows through the breaker, the 1200:5 CT will be carrying 12.5A current (2.5 times normal CT rating). Unless the CT has a thermal rating factor of 3, this is an unadvisable current for the CT to carry.

The next issue is that, when a bus fault occurs, the voltage across the open winding tap will be higher than the relay setting by a factor determined by the CT turns ratio. Figure 9 illustrates the concept. Assume a high impedance 87B relay is set to trip at 200V. For the Basler BE1-87B, the actual peak voltage at which the voltage clamping SCRs will turn on is $V_{SCR} = V_{SET} * 2 * Sqrt(2)$, or 566V. Since the relay is across the 1200:5 tap, the relay will start to turn on the SCRs at 566V, but some overshoot will occur in the 7 microseconds it takes to turn on the SCRs. Let us assume that 600V is reached. The voltage across the full 3000:5 winding will be 600*(3000/1200) or 1500V. Most CTs could handle this voltage level on a surge basis, but the standards on CTs are not actually written for this application. For instance, IEEE C57.13-1993, Section 6.7.1 states:
"Current transformers should never be operated with the secondary circuit open because hazardous crest voltages may result. Transformers conforming to this standard shall be capable of operating under emergency conditions for 1 minute with rated primary current times the rating factor with the secondary circuit open if the open-circuit voltage does not exceed 3500 V crest."

This effectively says that the CT internal wiring should be insulated to 3500V crest. The example above indicates there is plenty of margin below the 3500V, but one also must be aware that any wiring between the CT and the CT termination block might also see this peak voltage. In general, the issue of high voltage across the open windings is a concern that leads some to avoid ever using CT taps on high impedance bus protection schemes. If one is going to use taps on high impedance bus schemes, it may be a good idea to consult with the CT manufacturer on the CT insulation ratings and check that all wiring and terminal blocks are rated for the voltages that will be generated.

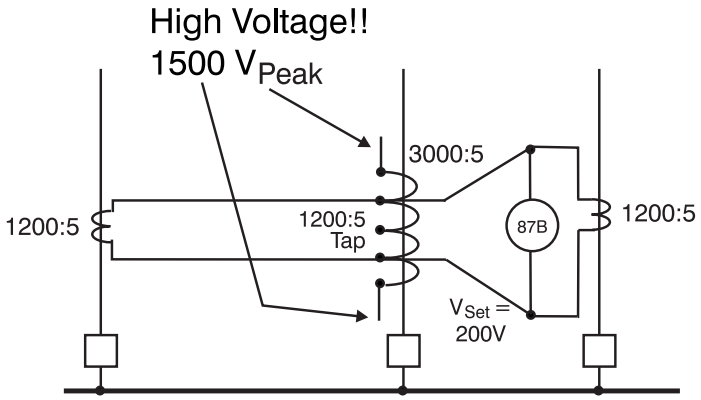

Figure 9: High Voltage on Open Terminals of a Tapped CT

2) Connect Two CTs on a Breaker in Parallel

An approach to effectively obtain a lower ratio out of the 3000:5 CT and not create as high a current in any CT is to connect two CTs in parallel. Some breakers have spare CTs, or the breaker can be ordered with extra CTs. Two 3000:5 CTs can be connected in parallel at their 2400:5 tap. The parallel CTs give a total current that effectively act as a 1200:5 CT.

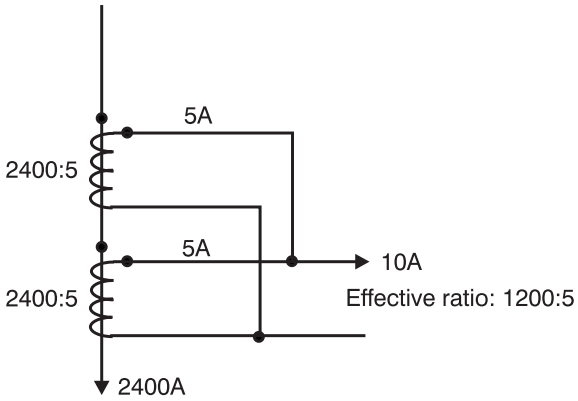

Figure 10: Paralleling CTs

3) Interconnect CTs at Taps (also called an Autotransformer approach)

A third approach is to connect the lower ratio CTs into the higher ratio CT at an appropriate tap, and then connect the 87B relay across the full higher ratio tap. The concept is best seen in fig. 11 below. The 87B monitors the higher ratio 3000:5 CTs connected across the full winding of the CTs. The lower ratio 1200:5 CT is connected into the appropriate tap of the higher ratio CTs. For instance, in the figure, the 1200:5 CT is connected to the 1200:5 winding taps of the 3000:5 CT. The interconnection of 1200:5 taps could also be extended to the other 3000:5 CTs so that several 3000:5 CTs are performing the transformation of the 1200:5 CT currents. This allows any one of the associated breakers to be taken out of service without disabling the bus protection scheme.

As an alternative to interconnecting CTs on actual breakers, a set of spare 3000:5 CTs can be purchased and mounted in a convenient location, and the interconnection would be done at these spare CTs. This removes concerns about what happens when a breaker is taken out of service and removes concerns about overloading of CTs, as discussed below.

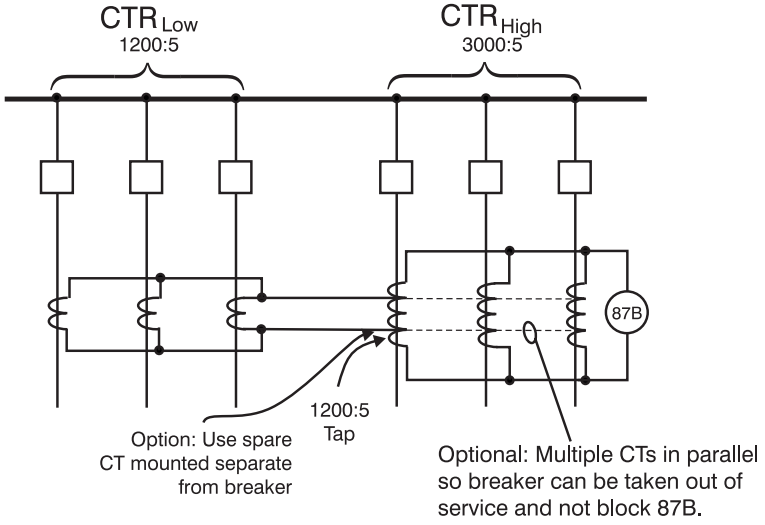

Figure 11: Paralleling Different Ratio CTs via Tap Connections

There is a problem with possible overloading of CTs when interconnecting CTs at their taps, that is just like the problem seen for connecting a 300:5 CT at 1200:5 and then running 300A through the CT. In fig. 12, the 3000:5 CT is carrying all of its current on the 1200:5 tap and is effectively connected as a 1200:5 CT. There is risk of the 1200:5 tap of the 3000:5 CT being driven at 12.5A. When using this scheme, one must consider the various operating contingencies to ensure that a CT will not be driven past its thermal rating factor. This issue can be bypassed if one employs the approach of using a spare set of CTs mounted separately from the breakers and specifies that this spare set of CTs has a sufficient thermal rating factor for the currents that will flow.

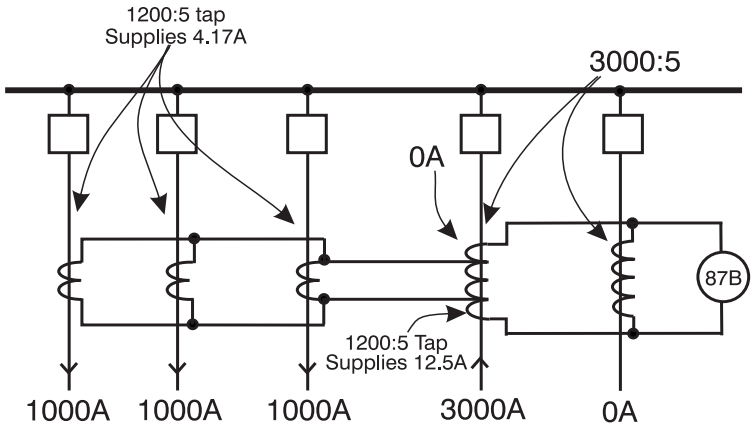

Figure 12: CT Overload Risk

The setting of the relay in this approach is very similar to the bus differential scheme with only one CT ratio. The concept is easiest to think through with the example in fig. 13.

- First, assume the 1200:5 CT on breaker 1 totally saturates and current is driven into the CT by the other CTs.
- Use I*R voltage drop calculations to determine the voltage at the 1200:5 tap of the 3000:5 CT. In this case, assume that we calculate 50V at the tap connection.
- Assume the 3000:5 CT operates ideally, and recall that the CT will also act as a voltage transformer in accordance with its turns ratio. The voltage at the full ratio of the tapped CT will be proportionate to the turns ratio of the CT in this case, 3000:5 / 1200:5 = 2.5, so voltage across the full CT will be 125V.
- Besides the voltage transformation, there is also a set of I*R voltage drop loss in the CT, so the actual voltage across the full winding of the CT will be a bit lower than predicted by the ideal equation. However, it is conservative to ignore this voltage drop, which results in calculating a higher voltage at the relay and a higher relay voltage setting. Since a higher voltage setting is more secure against misoperation, ignoring the tapped CT's I*R voltage drop aids in security.
- Next, continue with the I*R voltage drop in the leads at the second level (the 3000:5 section) of the CT string to determine what voltage will be seen at the relay. We might find 150V in this example, so it might be appropriate to set the relay at 150-200V.

If the CT on breaker 2 saturates, the issue is more complicated. You have two different current levels in the different parts of the CT winding and a complicated I*R voltage drop analysis. The voltage at the relay is still determinable with some thought.

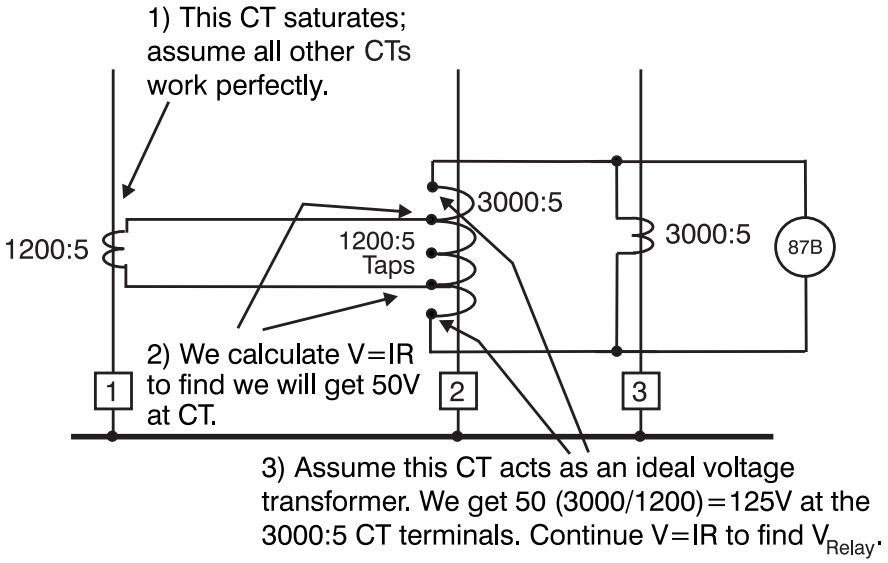

Figure 13: Relay Voltage for Saturated CT

Relay Design

There are two designs in use for high impedance bus differential relays. One design uses a non-linear impedance that begins to conduct current a bit more easily as the voltage at the CT summing point rises. The other design uses static switches (SCRs) that are turned on when CT secondary voltage rises above a set point.

Non-Linear Impedance Design

The current inputs of a high impedance bus differential relay present a non linear impedance to the CTs. For lower voltages the relay presents a high resistive impedance between the CT phase summation point and neutral, typically in the thousands of ohms range (typical simplified designs are shown in Figures 5 and 14 [3], [13]). Above some design voltage the impedance of the non-linear device begins to drop. Impedance never falls enough for the device to appear as a low impedance element, but typically as voltage rises much above 500V, impedance will drop to the range of 10-200 ohms, depending on the manufacturer's design and the specific voltage applied. The non-linear impedance serves to limit voltage at the relay during internal faults, but in some versions of the relay, current in the impedance is also monitored and is a secondary source of trip outputs. Due to the high impedance, CT saturation will occur during in zone bus faults, but the relay still is designed to trip.

The relay typically has a voltage and a current trip element in parallel. The voltage element will trip when a given voltage is detected and is typically tuned to fundamental frequency so that it will not be affected by DC or harmonics in the differential circuit. The current element trips when the current in the non-linear impedance rises above a given setting.

The non-linear impedance and other devices in the relay absorb substantial energy and can be damaged in a matter of cycles if fault conditions are not removed. Continuous ratings vary within the range of 150-250V, but internal faults and other conditions can create voltages well in excess of the continuous rating, including voltages above the CT knee point voltage. For this reason, bus lockout relays include contacts to short CT currents away from the bus relay.

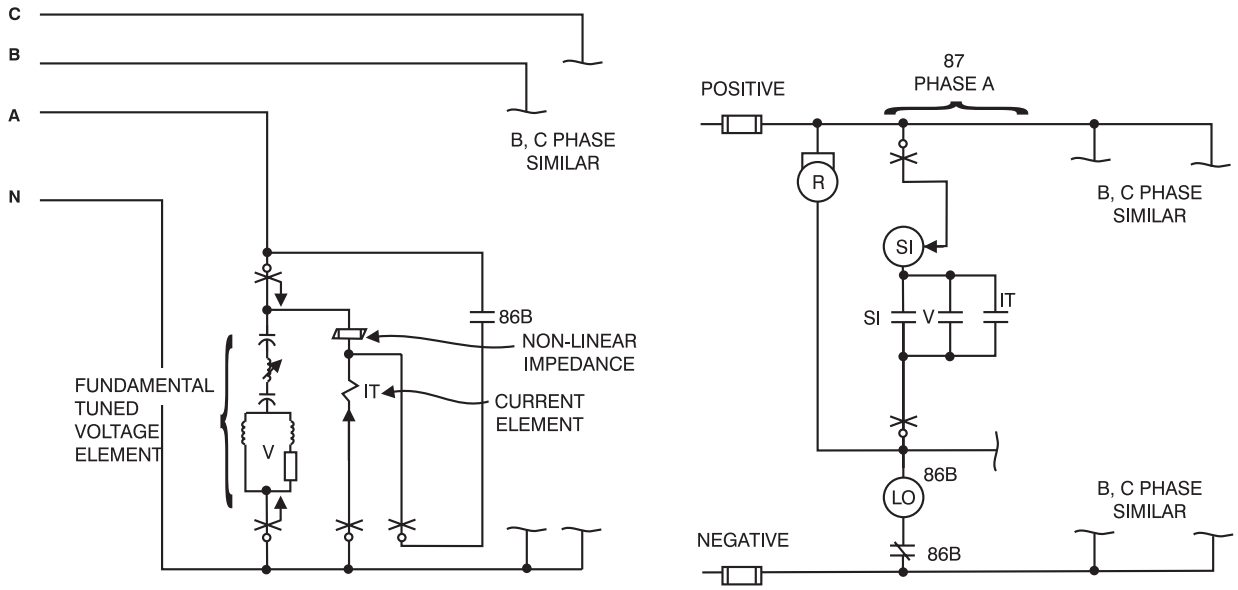

Figure 14: Internal Schematic, High Impedance Non-Linear Impedance Differential Relay [3]

Static Switch Design

Another design scheme for a high impedance differential relay has static switches/SCRs instead of the non-linear impedance arrangement. Its schematic is shown in Figures 15 and 16. In this design the static switches are off in normal circumstances. When voltages rise above a set level, the switches are turned on and are left on until the next current zero crossing. Once the switches are turned on, the relay presents a low impedance path to current. Once current flow is detected, the relay closes its trip contacts. Hence, it is actually a series operation of the voltage and current elements that leads to tripping. The voltage element monitors instantaneous voltage and is not tuned to the fundamental frequency. The effects of DC ofset are compensated for by the calibration of the unit.

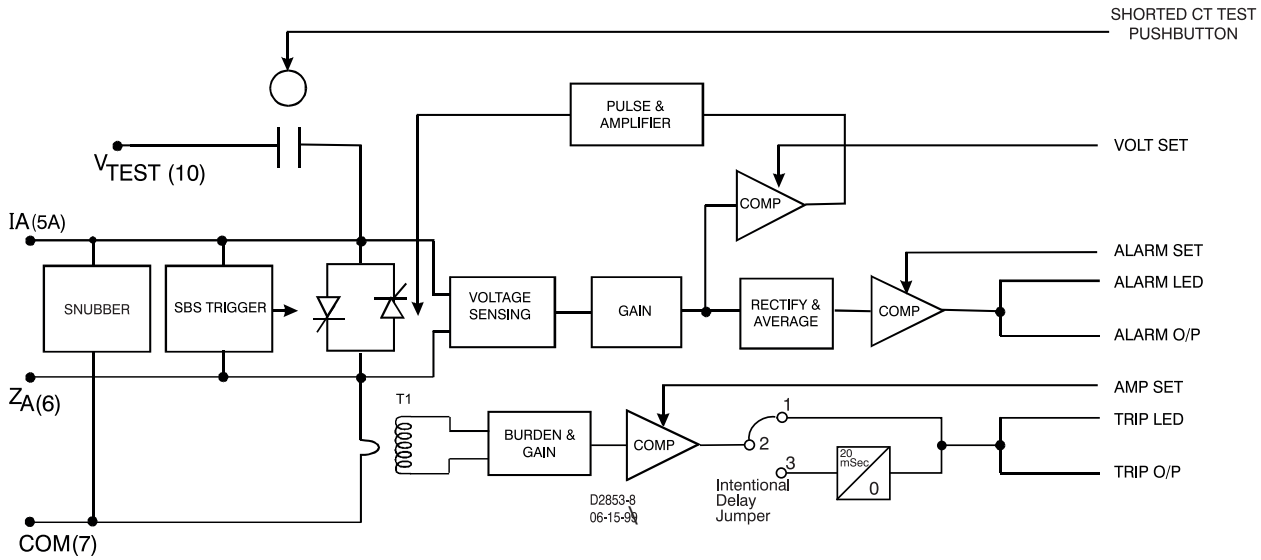

Figure 15: Block Diagram, High Impedance Static Switch Differential Relay [14]

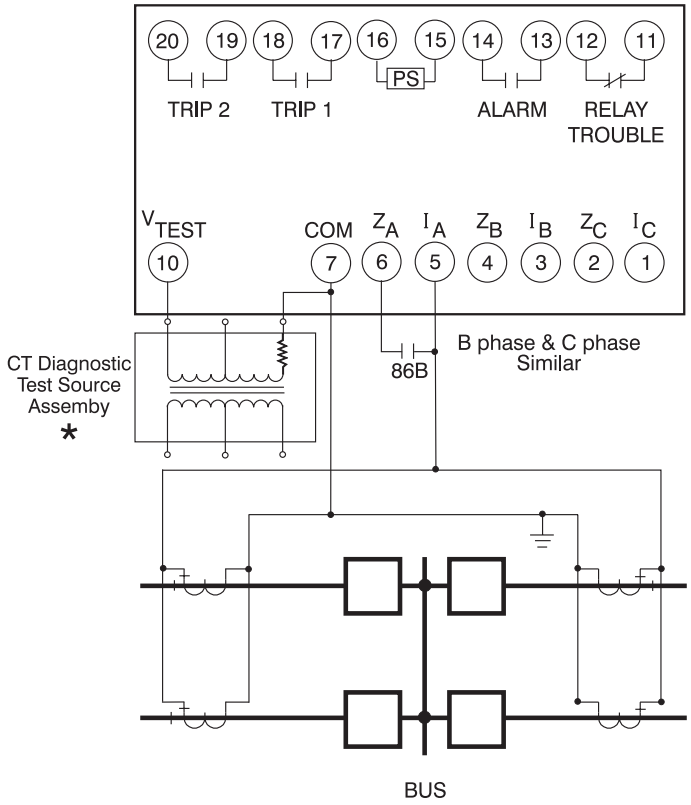

Figure 16: I/O High Impedance Static Switch Differential Relay [14]

Comparison of the Two Designs

The static switch approach is a series operation requiring two elements to operate for a fault to be declared (first voltage is detected, then current must be detected) compared to the parallel operation of the non-linear impedance design (which could operate on voltage or current detection alone). The series versus parallel arrangement tends to argue that the static switch design is, therefore, a bit more secure and the non-linear impedance design more dependable. An MTBF and failure mode analysis will be required to verify this.

As mentioned above, the voltage unit of the non-linear impedance design is tuned to the fundamental frequency, and the voltage unit of the static switch design looks at the instantaneous voltages. Tuning the relay to fundamental frequency inherently slows operation slightly. The effects of DC offset in the static switch design are accounted for in the calibration of the unit, and the relay is actually calibrated to trip at twice the relay's voltage setting when an RMS voltage is applied to account for worst case DC offset.

Operating times are in the range of 0.25 to 1 cycle for the static switch design. Operating times for the non-linear impedance design are in the range of 1 to 2 cycles. Operate times depend on settings and fault conditions and where in the same wave the fault begins, of course, and may be slower for low level faults. The high speed of the static switch design adds some justification that the tripping should be supervised by the current element. The design of one relay [14] allows for adding an intentional 20ms trip delay.

Maintenance / Testing

Due to the predominance of this type of bus protection, some discussion of the typical routine testing of the system is warranted. The two maintenance features described below may be seen in Figures 15 and 16 for the static bus differential relay.

Checking for High Impedance Connections, Turn-to-Turn Shorts, or Wrong Ratio CTs

After commissioning a bus differential circuit, it is possible that wiring will develop an impedance due to corrosion or other problems and will cause a voltage drop. This, in turn, causes a higher than normal voltage at the differential summing point. Also, CTs may develop turn-to-turn shorts that result in a differential error and an abnormal voltage across the differential summing point. It is possible that an improper CT ratio may not become apparent until loading becomes heavy or during a fault. These conditions can be detected by monitoring the voltage across the summation point of the CT. During equipment commissioning, check normal CT summation point voltage. This provides a reference against which to monitor voltage in the future or setting a voltage alarm. If the voltage at the relay rises above normal levels, an alarm can be sent. Note the alarm monitor output of the relay in figs 15 and 16.

Checking for Line or CT Short Circuits to Ground

A differential circuit could be left with a short from the CT to neutral (hence, bypassing the relay) for an extended period. This could have happened when a CT shorting bar was inadvertently left in place. Such a short will cause no immediate adverse effects and may go undetected indefinitely until the relay fails to trip. To check the CT circuit for a short to neutral without taking the bus out of service, a small voltage can be injected into the differential CT summation point while the system is in operation (or alternatively a small AC current injected). If voltage fails to be built, or if more than a small level of current associated with excitation requirements flows (or, in the case of current injection, the CT summation voltage does not rise), a short somewhere in the CT string is indicated. As shown in fig. 15, by pressing the test switch, a voltage is injected into the circuit. This should, in turn, cause an alarm level voltage to occur.

Non-Linear Impedance Integrity

The integrity of the non-linear impedance is critical to assure protection of the CT winding insulation. Relay testing programs should provide verification of their characteristics.

MEDIUM TO LOW IMPEDANCE UNRESTRAINED DIFFERENTIAL RELAYING

Basic Concept

This is an economical method of differential protection. As long as speed of operation is satisfactory and the proper installation guidelines are followed, the approach works well. The concept for a medium to low impedance differential relay is very similar to the concept for high impedance differential relaying. The major difference is that, instead of having a

high impedance voltage sensing relay in the differential circuit, a low impedance overcurrent relay is used with, in some cases, a “stabilizing” resistance placed in series with the overcurrent relay. The effect of the resistor is to equalize the apparent burden of each CT when currents are unbalanced and, thereby, reduce the differential current otherwise flowing through the relay as a result of unequal CT saturation. The resistor is chosen to force a secure current division between the relay and the saturated CT during the saturation of a CT during an external fault.

Adjustment of the overcurrent pickup allows some level of loading on the bus that is not included in the CT differential circuit (“unmonitored load” in the following discussion). The existence of loads without CTs feeding into the differential circuit is actually a form of the “partial differential” scheme to be discussed later but also covered here.

An advantage of using an overcurrent relay to monitor the differential current is that, because the impedance seen by the CT is low to moderate even during an internal fault, the application is more amenable to the use of auxiliary CTs and CT taps to compensate for those cases where full CT ratio cannot be easily made uniform at every breaker.

Relay Operation Analysis

The AC schematic in fig. 17 is basically a simplification of the high impedance relay circuit. The stabilizing resistance shown in fig. 17 may or may not exist and is discussed below. The analysis of how the system is configured and operated may be broken down to determine whether the stabilizing resistor does or does not exist.

To some extent, this type of relaying has two similar but notably different approaches to prevention of tripping during an external fault.

1) The overcurrent relay may be set to operate at high speed (i.e., with no intentional delay) when current rises above pickup if it is determined that the relay cannot pick up for an external fault. This application tends to use stabilizing resistors to prevent pickup during external faults or relies on CTs to only minimally saturate during external faults.

2) It can be set up to have time delayed tripping. It is anticipated that the relay will pick up for external faults, but some time delay is set into the relay to allow the relay to ride through the situation. This approach is more amenable to allowing loads that are not included in the CT summation scheme to be attached to a bus. The bus protection effectively becomes a ‘partial differential’ scheme in which the bus relay must have a pickup and a time delay set to coordinate with the protection of the unmonitored load.

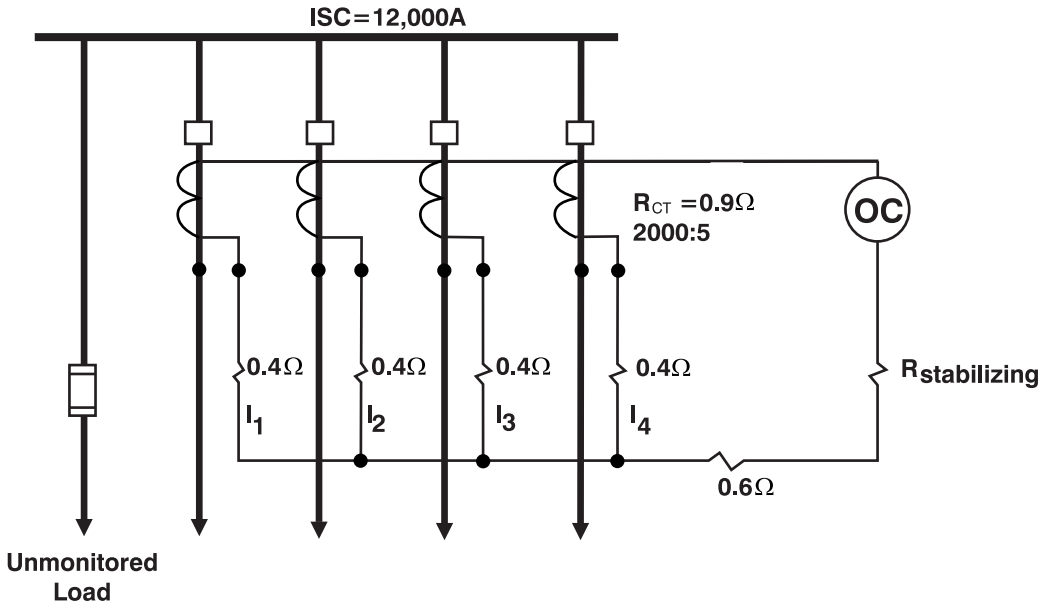

Figure 17: Low to Moderate Impedance - Unrestrained Differential Relay AC Schematic

CT SELECTION GUIDELINES

The CTs should be chosen so that all CTs have an AC voltage output rating greater than the steady state AC voltage seen by the CT during an external fault. The greater the margin used, the less likely that transient DC induced saturation will occur. If no AC saturation occurs for an external fault, and if there is no stabilizing resistor in the operate leg, then it is likely that the same system will experience little AC saturation during internal faults. During an internal fault, some AC saturation may be acceptable, since it is likely that the differential relay still will see enough current to force operation. If there is a stabilizing resistor, some level of AC saturation inevitably may occur, but this should be kept to a minimum. This is discussed further below.

Pickup Selection Guidelines

Some rules of thumb for setting the relay follow. These are, of course, quite flexible and easily may be bent. In the selection of the pickup, one should know whether the relay will respond to DC offset effects. The significance of DC offset, even if the CTs do not saturate, is that the currents in the relay will be increased. The example calculations below assume that the relay does not respond to DC offset, and DC offset is not included in the calculations.

Guidelines Applicable To Setup With and Without Stabilizing Resistors:

- Some ratios that may be good to try for are:

$$I_{pu} \le \left(\frac{I_{sc,min}}{3} \right)$$
$$I_{pu} = \left(\frac{I_{sc,max}}{8 \text{ to } 10} \right)$$
$$I_{pu} \ge \left(1.1 \cdot I_{unmonitored\ load} \right)$$

Eq. 18

(*unmonitored load = highest level of bus load not included in CT summation circuit)*

- Items 1 and 2 above are intended to help ensure fast operation for internal faults.
- Lower pickup makes the system more sensitive to and able to operate faster for internal faults.
- Higher pickup helps coordination with fuses protecting any unmonitored load.
- Higher pickup helps keep the relay from responding to moderate levels of CT saturation during external faults.

Additional Guideline When Using Stabilizing Resistors

- Higher pickup allows the use of a lower stabilizing resistance, yielding lower CT saturation during internal faults and lower resistor watt ratings.
- If using a stabilizing resistor, to ensure that the relay will operate quickly even if the CTs go into saturation during an internal fault:

$$I_{pu} \le \left(\frac{1}{3} \frac{V_{CT\ rated}}{R_{stab} + R_{operate\ circuit\ wire\ resistance}} \right)$$

Eq. 19

Additional Guideline When Not Using Stabilizing Resistors

- If it is determined that there is low risk of CTs going into saturation during an external fault (e.g., after using equation 10) and a stabilizing resistor is not required, the minimum pickup should also be considered based on some low level of CT error. A possible approach may be to assume 5 to 10% error from the CT closest to the fault during an external fault.

$$I_{pu} \ge (0.05\ to\ 0.10) \cdot I_{sc,max}$$

Eq. 20

Assuming the analysis (that there was no risk of CT saturation) was correct, then if current is seen above this level, we may trip instantly, for it must indicate an internal fault.

Example System

Suppose, for the example, there is 75A of unmonitored load, a minimum bus fault duty of 5000A, and a maximum of 12000A. Applying Eq. 18:

$$I_{pu} \le \left(\frac{I_{sc,min}}{3} \right) = \frac{5000}{3 \cdot 2000{:}5} = 4.167\,A$$

$$I_{pu} = \left(\frac{I_{sc,max}}{8 \text{ to } 10} \right) = \frac{12000}{(8 \text{ to } 10) \cdot 2000{:}5} = 3.0 \text{ to } 3.75\,A$$

$$I_{pu} \ge \left(1.1 \cdot I_{unmonitored\ load} \right) = 1.1 \cdot \frac{75}{2000{:}5} = 0.21\,A$$

The CT rating is about 200V. Looking forward to calculations on the following pages, we will find a stabilizing resistance of 14Ω. Applying Eq. 19:

$$I_{pu} \le \left(\frac{1}{3} \frac{V_{CT\,rated}}{R_{stab} + R_{operate\ \ circuit\ wire\ resistance}} \right) = \frac{1}{3} \frac{200}{14.0 + 0.6} = 4.6\,A$$

To complete the exercise, in the event one did not install stabilizing resistors because one did not anticipate any saturation but wanted to allow 5-10% error in one CT, and applying Eq. 20:

$$I_{pu} \ge (0.05\,to\,0.10) \frac{12000}{2000:5} = 1.5\,to\,3.0\,A$$

From all this, let's choose 3.5A.

Using Stabilizing Resistors to Prevent Misoperation For External Faults

A stabilizing resistor should be considered if one has determined that the CTs are at risk of going into saturation for an external fault or there is no time delay in tripping. If there is no CT saturation risk or there is relay time delay to ride through transient CT saturation, then the material below may be skipped, but it may be a good practice to consider including the resistance in most installations.

Stabilizing Resistors/Reactors

In many applications, as shown in fig. 11, the security against operation for an external fault will be improved by adding a stabilizing resistor in series with the overcurrent relay in the differential summation leg. The resistor changes the current division during CT saturation so that more current of the in-feeding lines circulates in the saturated CT of the faulted line instead of the overcurrent relay. The discussions to follow provide insights into when the resistor will be beneficial.

To avoid the heat dissipation problems associated with resistors, the stabilizing resistance could be a reactor. One application is to use a saturable reactor. Under voltages across the reactor of less than possibly 25 Vac, impedances are relatively high, in the range of 30Ω or more. However, if AC voltage across the reactor rise above the reactor's knee voltage, the

AC impedance becomes the reactor's air core impedance, possibly on the order of 3Ω , with some internal winding series resistance, likely a small amount. However, a reactor's impedance under the application of DC offset will be difficult to analyze. 1) Saturation of the reactor may occur very quickly under a DC voltage, and 2) even if the reactor does not saturate, current in a reactor rises exponentially as long as the DC voltage is applied. To compensate when using a reactor, the overcurrent relay must have a time delay greater than two to four times the system L/R time constant in order to ride through the DC offset problem. This paper only considers adding a resistor; evaluation of adding a reactor lies with the person considering it.

CT Saturation Equivalent Circuit

Deciding on the resistance requires an equivalent circuit for the saturated CT. Assume again that the external fault causes saturation of the nearest CT and that all other CTs do not saturate. Noting that the stabilizing resistor may or may not exist, the equivalent electric circuit will be:

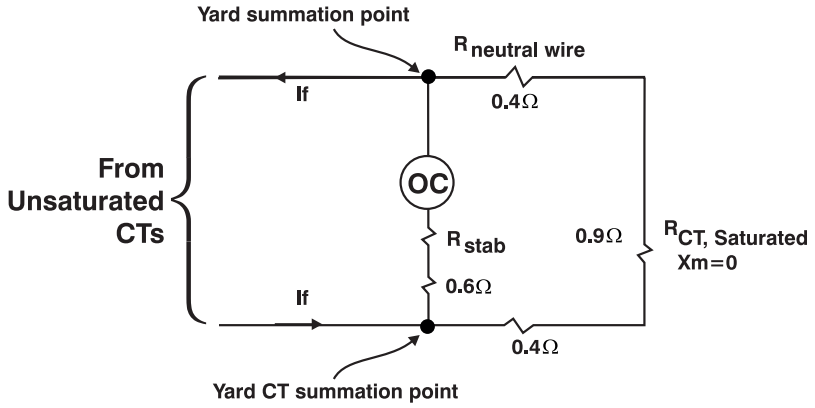

Figure 18: Low Impedance Diff., Equivalent Ckt For CT Saturation During An External Fault

Resistance Selection

A conservative selection for the resistor is made by dividing relay "open circuit voltage" during the CT saturation condition by the relay pickup current setting. To find the open circuit voltage, pretend that the overcurrent relay circuit branch is an open circuit and find the voltage that will develop across the open circuit as current is forced through the saturated CT by the remaining CTs. Again, it is the line-to-ground fault that has higher lead resistance because current must flow in the neutral leg, so a line-ground fault is assumed in this example.

$$V_{max,ct\ sum\ point} = \frac{I_{sc,max}}{CTR}\left(R_{ct} + 2 \cdot R_{wires}\right) \qquad \text{Eq. 21}$$

$$= \frac{12000}{2000{:}5}(0.9 + 0.4 + 0.4) = 30A \cdot 1.7\Omega = 51V$$

The 3.5A pickup in this example yields a stabilizing resistance of:

$$R_{stab} = \frac{V_{open\,circuit}}{I_{pickup}} - R_{operate\,circuit\,wire\,resistance} = \frac{51V}{3.5A} - 0.6\Omega = 14.0\Omega \quad \text{Eq. 22}$$

Once a resistor has been chosen, the current division between the differential leg and the saturated CT can be found and checked to determine how secure against misoperation the resistor selection has made the system :

$$I_{relay} = I_{sc}\frac{R_{sat\,ct\,circuit}}{R_{sat\,ct\,circuit} + R_{operate\,circuit}} = \left(\frac{12000}{2000:5}\right)\left(\frac{0.9+0.4+0.4}{(0.9+0.4+0.4)+(14.0+0.6)}\right) = 3.13A \quad \text{Eq. 23}$$

This is around 11% below the pickup of the relay. The system is a bit more secure than apparent if it is considered that the saturated CT will produce at least some voltage, and, hence, the voltage at the summing point will not be quite the calculated 51V. The system is less secure than apparent if the relay responds to DC offset, or the max fault current and line impedances used in the calculations were off by only 11%. If desired, pickup current or resistance can be raised to improve security.

Resistor Watt Rating

To prevent resistor damage, it may be good for the resistor to be able to withstand the condition of continuous current just below the relay pickup. The watt rating will be:

$$WattRating \geq I_{relay\,pu}{}^2 R_{stab} = 3.5^2 \cdot 14 = 172W \quad \text{Eq. 24}$$

The resistor short time power absorption during internal faults must also be considered. A rule of thumb is that a wire-wound resistor can withstand overloading according to the following equation:

$$W_{short\ time} = W_{rated}\frac{50}{t} \quad \text{for } 1 \leq t \leq 25 \quad \text{Eq. 25}$$

(source: telecon with Dale Resistor engineer). Note this rule allows loading a resistor at 50 times its rating for 1 second, and the maximum short time loading is at the 1 second rate. Assuming the worst case internal fault pushing 30A (=12,000/2000:5) into the resistor for a maximum of 1 second yields:

$$WattRating \geq \frac{I^2 R_{stab}}{\frac{50}{t}} = \frac{30^2 \cdot 14}{\frac{50}{1}} = 252W \quad \text{Eq. 26}$$

In this case the second test was the worst case, but in substations with high relay pickup current or low fault current, the first test may be worst case.

Using Time Delays to Prevent Misoperation For External Faults

If relay pickup due to DC effects cannot be ruled out and a stabilizing resistance is not desired, time delay in the relay may be used instead. The main reason to delay tripping is to allow time for DC offset induced saturation conditions to die out, allowing a better analysis of whether there is truly a bus fault.

A bus with an X/R ratio of 10 at 60 Hz has an L/R time constant of $10/(2\pi f) = 0.0265$ seconds or 1.6 cycles. The saturation waveform in the CT takes 2 to 4 time constants to decay to a fairly normal current waveform. Hence, not much time delay is required; in the range of 0.10-0.15 seconds should supply sufficient delay in most cases. Delays longer than this may result in remote line relays tripping for a true bus fault.

A rule of thumb is to set the relay time dial so that, with the time delay at maximum bus fault current, the relay delay should be greater than two to four times the system L/R time constant, typically in the range of 0.10-0.15 seconds (6-9 cycles at 60 Hz), and utilize a curve with a relatively flat time/current characteristic. This curve keeps the time delay to a minimum at lower fault currents.

Using the earlier example, with a 2000:5 CTR, a 3.5A pu (=1400A primary), and a time dial of 3 on a Basler Electric S2 curve, we trip in 0.1 seconds for a 12000A bus fault, 0.12 seconds for a 5000A bus fault, and 0.3 seconds for a 2000A bus fault.

If coordinating with a downstream device fuse; (e.g., an unmonitored, fused load on the bus) delay has to be greater and a very inverse or extremely inverse curve likely is required. Similarly, the pickup setting is driven by local relaying coordination.

Operation During an Internal Fault

During an internal fault, the full substation fault duty is impressed through the relay. If there is no stabilizing resistor, AC induced saturation is usually low. If there is a stabilizing resistor, voltage across the resistor may be high, which will tend to drive the CT into AC saturation. Assuming no saturation:

$$V_{summation\,point,no\,saturation} = \frac{I_{sc,rms}}{CTR}(R_{stab} + R_{relay\,circuit\,wire\,resistance}) = \frac{12000}{400}(14 + 0.6) = 438V \qquad \text{Eq. 27}$$

It appears from this analysis that the CT actually will go into saturation, since 438V is much greater than the C200 voltage rating of our CT. The depth of saturation is defined to a large extent by the stabilizing resistance, which was in turn defined by the relay pickup. A higher pickup reduces the required resistance of the stabilizing resistor (Eq. 22).

However, the risk of a CT entering into low to moderate saturation during an internal fault may be quite acceptable. What is the response of the relay for a distorted waveform from a partially saturated CT? What fundamental current does the CT produce? Will there be

enough secondary current to cause the relay to trip? A CT driven into saturation produces a “spiky” harmonically rich wave form, similar to the first few cycles of Figure 4. A fairly conservative approach to verifying that the relay senses the fault is to assume that the relay sees the effective secondary current as reduced proportionately to the level of attempted saturation times the maximum current at no saturation. For instance, assume a CT rated at 200V secondary and assume a burden of 10Ω. For this circuit, in steady state conditions (i.e., negligible DC offset), the CT can push about 20A into the secondary with no saturation. Now assume, as in the above analysis, that the primary current is twice as high and tries to drive the secondary voltage to 400V. A conservative approach is to estimate that the current sensed by the relay will be about 20A*(200V/400V) or 10A. This approach can be used to determine if the saturated CT under steady state conditions pushes enough current into the overcurrent differential circuit to cause a relay operation. For our circuit, the maximum current that the CT can push into the secondary with no saturation is:

$$I_{ct,Vrated,sum.point} = \frac{V_{ct,Vrated}}{R_{stab} + R_{relay\,circuit\,wireres.}} = \frac{200}{14 + 0.6} = 13.7A \qquad \text{Eq. 28}$$

This is about four times the pickup of the relay. Considering the approach to saturation effects described above, the relay senses current at about two times pickup (4*200V/438). Note this is a conservative approach and the relay likely sees much more than two times pickup current. Even as the CTs saturate, the relay should sense enough current to operate reliably.

The minimum operate current, of course, is:

$$I_{min} = CTR \cdot pickup = 2000{:}5 \cdot 3.5 = 1400A$$

which is according to our design specification in Equation 18.

LOW TO MODERATE IMPEDANCE RESTRAINED DIFFERENTIAL RELAYING

Basic Concept

The low impedance restrained bus differential scheme is similar in concept to the familiar transformer restrained differential relay, and some companies have used a transformer differential relay for this application. There are through current restraint quantities and differential operate quantities. The restraint and operate windings interact so that the higher the through current level, the higher the required operate current. But in the bus relay the restraint and operate circuit may be simpler, the restraint slope may be fixed, the CT tap adjustment system may not exist, and the harmonic restraint may not exist.

The operate circuit may contain some impedance. This adds some security against operation during the poor performance of a CT. The concept is similar to that described for the use of stabilizing resistors for low impedance unrestrained differential relaying, previously described.

Multi-Restraint Design

The most involved version of this concept has all CT signals brought into the relay individually into separate restraint windings before being summed together for the operate circuit as shown below. Individual tap adjusts may or may not exist on each input.

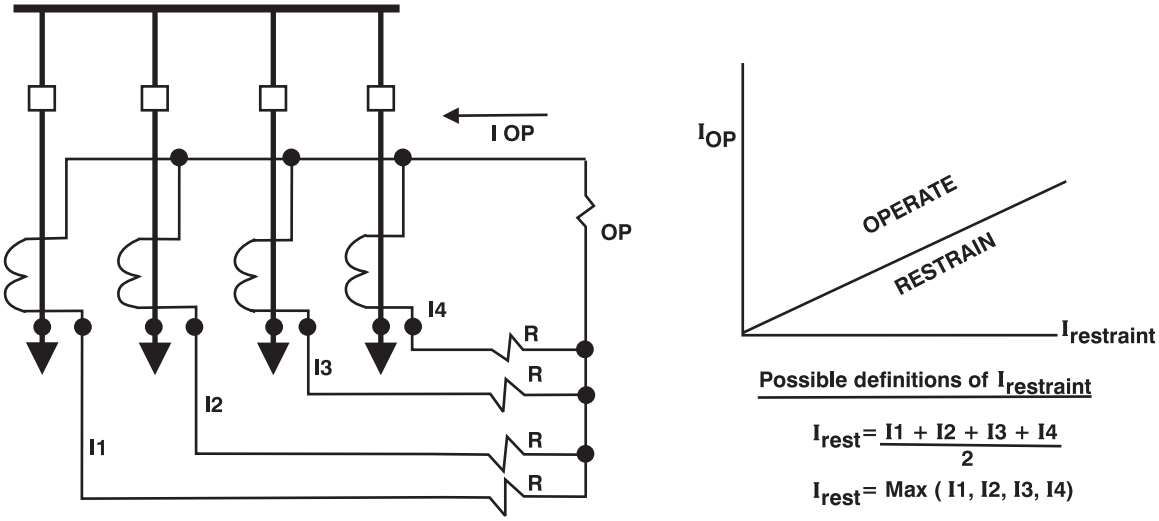

Figure 19: Multi-Restraint Bus Differential Schematic

Transformer differential relays are sometimes used for this type of bus protection. Sometimes questions arise about how to set a transformer differential relay when used for bus protection.

Transformer differential type relays have little means to differentiate between an internal fault and the absolute and complete saturation of a CT during an external fault. The assumed worst case complete saturation of a CT during an external fault looks identical, to the relay, to an internal fault where the breaker was not supplying any current (e.g., breaker was open). For these relays to be secure against operation for an external fault, there must be some assumption of CT performance for an external fault. There are three approaches: either slow down the relay operation so that transient DC saturation can be ridden through, use CTs robust enough to only slightly go into DC induced saturation, and combined with these, the third approach of setting the relay to not operate for some lower level of CT saturation.

Two compensating factors are: 1) the complete saturation of a CT is not a true phenomenon, and current wave forms similar to fig. 4 are more realistic. This wave form has some current component that will help restrain the relay from operating, 2) the relay typically takes a finite time to decide to trip, which allows time for DC induced saturation to decay and 3) many differential relays only respond to error in fundamental frequency current, so the worst effect of CT saturation is filtered out.

CT Selection

Just as when using an overcurrent relay, the CTs should be chosen so that all CTs have an AC voltage rating greater than the steady state AC voltage that will be seen by the CT during an external fault. The greater the margin that is used, the less likely that transient DC induced saturation will occur. If harmonic blocking is used, as described below, then it is important that no AC saturation should occur during an internal fault either, because the harmonic blocking may prevent relay operation during an internal fault if AC saturation is occurring.

CT Pairing

Any ource to a bus should be on its own transformer restraint winding. It is sometimes the practice, especially in distribution substations, to sum CTs together rather than bring each CT into individual restraints in the relay. This is shown in fig. 20, where a transformer differential relay wraps a bus as well as a transformer. If this is done, the user should be aware that, for the external fault shown in the figure, the current path indicated in I_1 in the figure presents a large through-current restraint. But if there were a source on one of the adjacent feeders, or if a bus tie is feeding the bus, as indicated by current path I_2, the relay sees only the CT error and no through-current restraint, so the relay will have a greater tendency to operate for CT saturation.

Slope

Some allowance for partial CT saturation may be accounted for by adjustment of the slope. Slope sets how much operate current must exist for a given restraint current before a trip is issued. Slope and restraint are calculated variously from one relay manufacturer to the next, so specific guidelines are difficult to offer. In Figure 17, restraint current is shown as a variant of the average of the restraint currents, but another manufacturer may define restraint as the maximum restraint current. It is suggested that the relay slope be set so that at some moderately high error, for example 20%, of the CT closest to the external fault, the relay is restrained from operation. For instance, assume the relay had the operation characteristics such that:

$$I_{restraint} = Max\,Magnitude\left(\frac{10}{5},\frac{10}{5},\frac{10}{5},\frac{-24}{5}\right)=\frac{24}{5}=4.8A_{pu\,tap}$$

$$I_{operate} = Summation\left(\frac{10}{5}+\frac{10}{5}+\frac{10}{5}+\frac{-24}{5}\right)=1.2A_{pu\,tap} \qquad \text{Eq. 29}$$

Assume an external fault on line 4 with correct operation of the line 1, 2, and 3 CTs, and partial saturation of the line 4 CT. Assume 10A secondary from the secondary of the CTs on lines 1, 2, and 3 (into the bus) and 24A secondary (20% error) from the secondary of the CT on line 4 (out of the bus). Assume all taps are set at 5A. The restraint and operate current would be:

$$I_{restraint} = Max\,Magnitude\left(\frac{I_1}{tap1}, \frac{I_2}{tap2}, \frac{I_3}{tap3}, \frac{I_4}{tap4}\right)$$

$$I_{operate} = Summation\left(\frac{I_1}{tap1}, \frac{I_2}{tap2}, \frac{I_3}{tap3}, \frac{I_4}{tap4}\right)$$

The ratio calculated by the relay would be:

$$Ratio\frac{I_{op}}{I_{rest}} = \frac{1.2}{4.8} = 25\% \qquad \text{Eq. 30}$$

This says that if the relay slope is set less than 25%, the relay would trip, and if slope is set greater than 25% the relay would be restrained from operation.

Minimum Operate Current

A possible approach to setting the minimum sensitivity is as follows. First, select a minimum fault for which one wishes the relay to operate. Selection is not critical. Just choose a value well below minimum bus fault duty so that the relay operates fast for a bus fault, and avoid going so low false operation due to extreme sensitivity becomes a concern. Assume, for instance, that one wishes to trip for a 500A fault on the bus, have CT ratios of 2000:5, and is using taps of 5A. A fault of 500A will yield a per unit operate current of:

$$I_{PU} \geq \frac{500}{2000:5}\left(\frac{1}{5}\right) \approx 0.25$$

Hence, setting the relay to 0.25 per unit tap minimum operate will allow the relay to trip only for faults >500A, in this example. Note that, for operation, the slope setting adds an additional requirement that:

$$I_{op,pu} \geq I_{restraint} \cdot Slope$$

(noting that restraint and slope calculations are manufacturer specific) so required operate current will be higher for through faults.

Harmonic Restraint

Depending on manufacturer design, transformer differential relays are characterized by restraint of operation if substantial 2nd or 5th harmonic currents are detected in the operate element, and this quantity is sometimes adjustable. This feature is intended for the detection of transformer inrush current, but it has some use in bus protection. A saturating CT will produce a reduced fundamental component and current with a notable harmonic content. This will result in an operate quantity in the relay with both a fundamental and a harmonic content. By setting the harmonic restraint so that a low level of harmonic current will block operation, it is possible to reduce the risk of operation of the relay to CT saturation.

If harmonic restraint is used, it must be assumed that there is no steady state saturation during an internal fault. If steady state AC saturation does occur, then harmonic restraint may continuously block tripping.

Time Delay

If the relay has the ability to add an intentional additional delay to the tripping time, and if system stability is not an issue, it may be helpful to add a small time delay to the trip output to allow the relay to ride through transient DC induced saturation. The total time delay to fault clearing, including all relay delays (fault detection time delays plus intentionally added time delays) plus breaker operate time, must not be greater than any remote relays that may be timing towards trip. Most commonly will be the zone 2 time delays of remote line relays (typically 0.3 - 0.5 seconds). A suggested time delay for the bus relay may be twice the system time constant. Note that:

$$1\ \text{Time Constant} = \frac{L_{sys}}{R_{Sys}} = \frac{X_{sys}}{2\pi f\ R_{sys}} \qquad \text{Eq. 31}$$

For an X/R = 10 and t=60, one time constant is about 0.0265 sec., so 2 time constants equals 0.053 seconds.

Unrestrained Trip

The unrestrained trip will ignore the harmonic restraint when differential rises above the setting (usually in multiples of tap). It is typically a very fast function (0.5-1.5 cycles). It is suggested that the unrestrained trip be set at some level comfortably under the maximum bus fault level (maybe 75% of the maximum bus fault).

$$\text{Unrestrained Trip} = 0.75\frac{\frac{I_{max\ sc}}{CT_{ratio}}}{tap} \qquad \text{Eq. 32}$$

For the example system being used here, this comes to:

$$\text{Unrestrained Trip} = 0.75\frac{\frac{12000}{2000:5}}{5} = 4.5\ \text{multiples of tap}$$

Overlapping Bus and Transformer Protection

Similar to this application, another bus protection scheme wraps the bus by the transformer differential relay. Due to the need to compensate for transformer inrush, magnetization current, and uncertain transformation ratios, this approach is inherently lower in sensitivity compared to a dedicated bus differential relay. However, since bus faults are typically high in magnitude, this normally is not a problem.

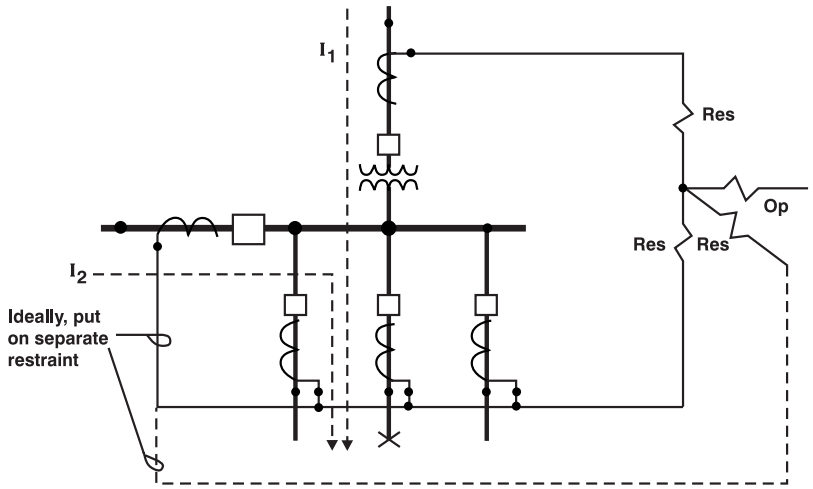

Figure 20: Multi-Restraint Bus Differential Schematic - Transformer Differential Wrapping Bus

The pairing of CTs presents the possibility that through current may present no restraint current to the relay, as observed by comparing what the relay sees for fault current paths I1 and I2.

Electromagnetic Restraint Design

In classical electromagnetic relay design it is difficult to design a relay with numerous restraint circuits. This tends to limit the number of restraint circuits, and in one common design the limitation is 6 restraint circuits, which means that CTs are judiciously summed together in the field before being brought into the relay.

The relay relies on opposing magnetic torque on an operating arm to create the restraint to operation. In the 6 input version of the relay the restraint coils consist of three pairs of restraint circuits, with each pair on its own magnetic core. With two windings on a common magnetic core, the paired currents can either add or subtract magnetically. For instance, two in phase restraint currents of 5A might subtract to create no restraint or might add to create 10A effective restraint, depending on the way the relay is wired. This creates difficulties as well as flexibility and, hence, the relay manual supplies special instructions on the proper use and configuration of the restraint windings.

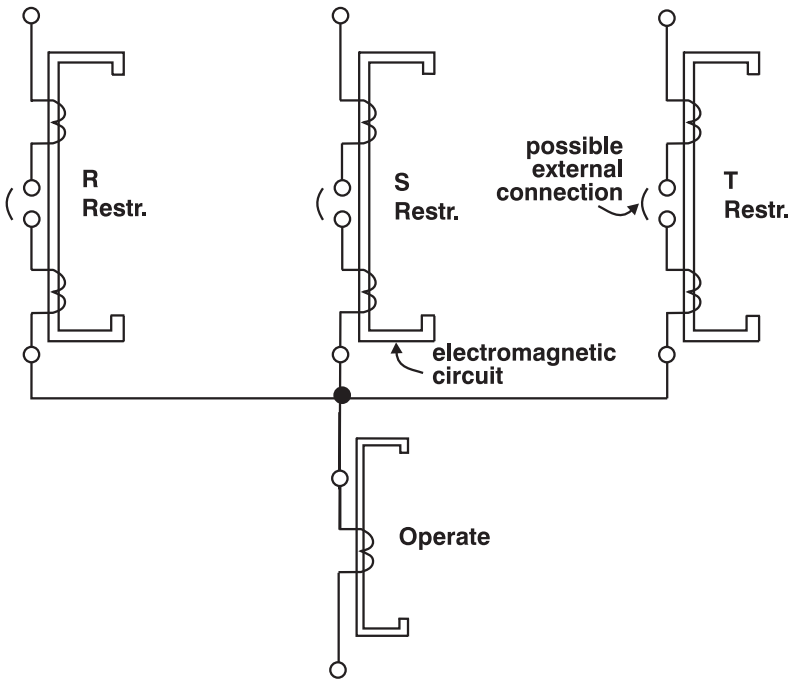

Figure 21: Electromagnetic Restrained Bus Differential Relay

Rectified Current Comparator Restraint Design

Several solid state relays use a rectification scheme to create operate versus restraint currents, as seen in fig. 22. In this scheme the current from each CT is brought into a rectifier arrangement as shown. If the net current on each CT sums to zero, then no current flows in the operate circuit. Note: In this figure no input auxiliary CT is shown.

This design typically does, however, have auxiliary CTs, sometimes one for every input current, to adjust input currents to a level the electronics can use. Note also the optional stabilizing impedance used in some designs which serves a similar purpose as in the unrestrained overcurrent differential design.

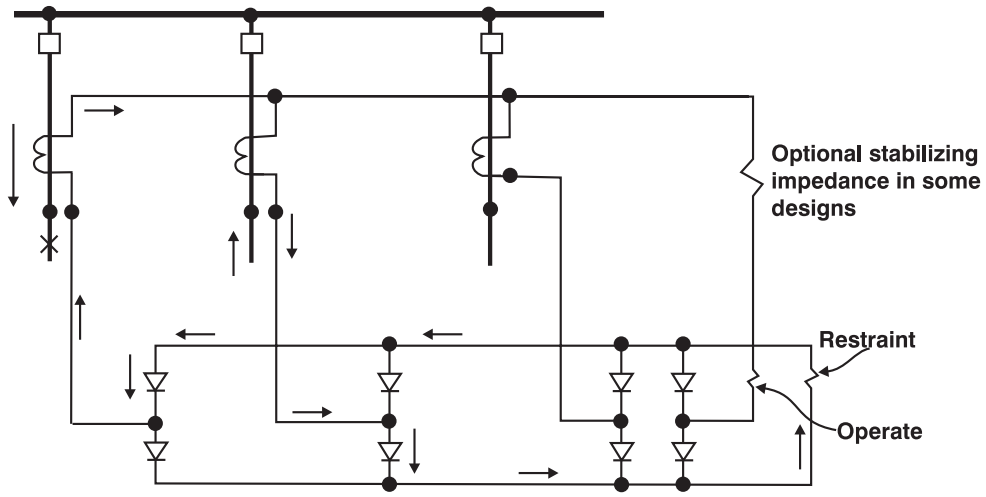

Figure 22: Rectified Current Comparator Conceptual Design

Speeds of the rectified AC type are in the 1/2 cycle range, being as fast as a high impedance static switch bus differential relay. The application typically has few settings requirements and they tend to be fairly specific to the relay manufacturer's design. Some settings include a stabilizing resistance for the operate circuit and a minimum operate current pickup level. The manufacturer's instruction manuals should be consulted for details.

Advantage of Monitoring Each CT

An advantage of monitoring each CT input individually, as is done in several of the last designs reviewed, is that the application is more amenable to the use of auxiliary CTs and CT taps to compensate for those cases where full CT ratio cannot easily be made uniform at every breaker. It also allows each CT to be monitored for other purposes, such as breaker failure detection.

Another advantage of monitoring each CT is that it allows the relay to monitor for CT saturation. CT saturation has wave form signatures used by some advanced differential relays to intelligently decide if the fault is inside or outside the zone of protection, even in the presence of saturation, and some advanced bus protection schemes have been marketed using this scheme.

The disadvantages of monitoring each CT are a) higher relay cost, and b) since the CT circuits are brought all the way back into the control room, the burden seen by the CT during external faults is higher compared with those applications where CTs are summed in a yard subpanel. This higher impedance increases the tendency of the CT to saturate during external faults.

INTERLOCKED LINE AND TRANSFORMER RELAYING

Basic Concept

In this design there is actually no dedicated differential relay but the logic derived from an array of relays in the vicinity of the bus. There are two main categories of the application. In a radial distribution application, if a bus overcurrent relay sees a high level fault but no feeder relay sees a fault, it might be assumed that there must be a bus fault. Similarly, in a transmission application, if all equipment on the bus relays see a fault in the reverse direction, it might be assumed that there is a fault on a bus.

Radial Application: Instantaneous OC Relays with Delay

In the typical radial distribution application, current flows outward from the transformer to the bus, then to the various feeders. It is fairly easy to see that, if there is a bus fault, current flow will only be seen by the bus overcurrent relay. Hence, an instantaneous bus relay with a small time delay and a circuit to block operation if a downstream relays sees a fault, can be used to monitor for a bus fault. The AC and DC schematic is shown in fig. 23.

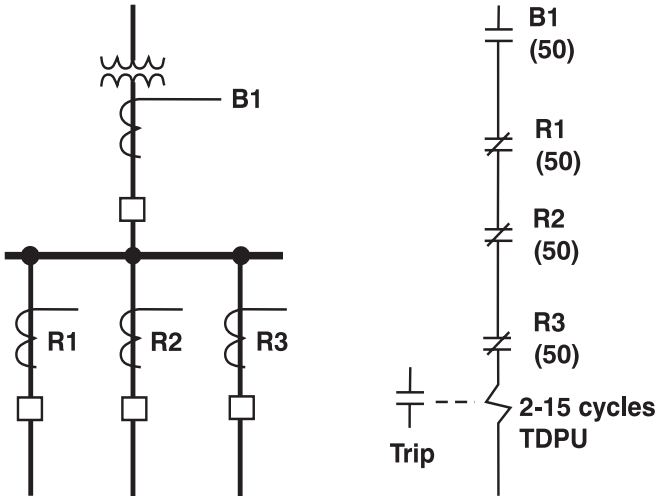

Figure 23: Distribution Interlocked Bus Protection Schematic

The time delay required in the bus relay output contact is likely in the range of 2 to 15 cycles. The delay varies according to the design of the feeder relays. It depends on how fast one expects the block to be generated by the feeder relay and propagated through any interposing logic element.

Transmission Application: Directional Relays

The scheme for a transmission application is similar to the radial substation relay interlock scheme. There are two logic schemes that could be used, one more secure, the other more dependable. Both applications have the advantage of being able to be performed, in many cases, with existing relays, especially the more dependable scheme.
Each method below requires some thought about how operation will be affected when one

of the relays in the logic scheme is taken out of service or a breaker is open. If not properly considered, a permissive taken out of service may block the scheme from operation, and if a blocking relay is taken out of service, a misoperation may occur.

However, due to the complexity of the design and the reliance on so many separate relays to perform correctly, neither scheme is very commonly used. Also, the secure scheme tends to require unavailable protective relaying elements in the line relays (at least until the advent of multifunction microproessor based line relays) and the more dependable scheme tends to have security questions and time delay problems.

More Secure Scheme

The more secure scheme requires that every breaker on a bus has protective relaying capable of closing a contact when it sees a fault behind itself. The logic is shown in fig. 24. The logic is similar to what a transmission protection engineer refers to as a line POTT scheme. Since every relay must sense the fault, it may be considered a fairly secure arrangement.

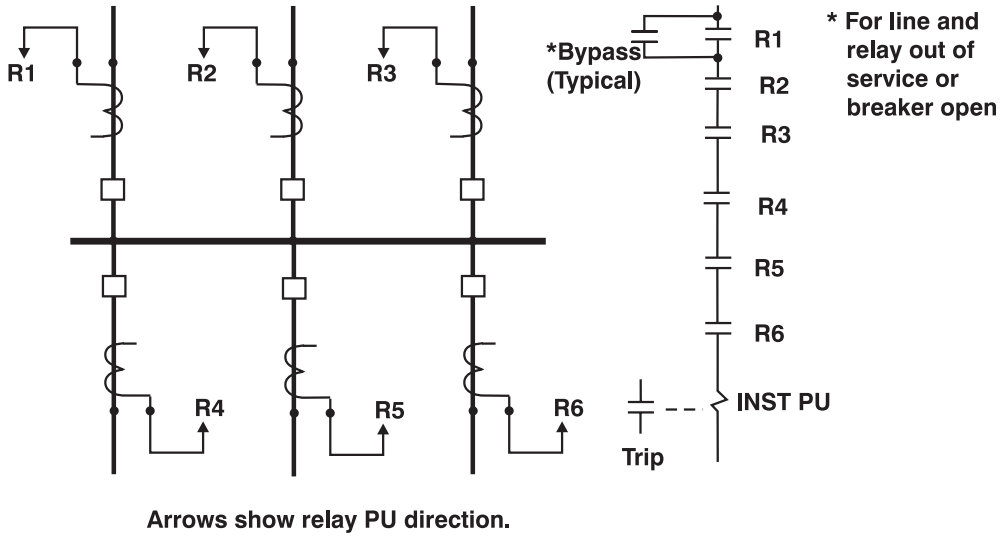

Figure 24: Transmission Interlocked Bus Protection Schematic, Secure Scheme

More Dependable Scheme

A more dependable approach has a logic similar to that of the radial substation logic, but it also tends to be less secure and slower. This scheme tends to be more amenable to use with existing line relays. As a minimum, it requires only one relay that looks into the bus, with tripping blocked if any other relay sees a fault beyond the bus. The blocking elements must reach farther out onto the line than the relays looking into the bus.

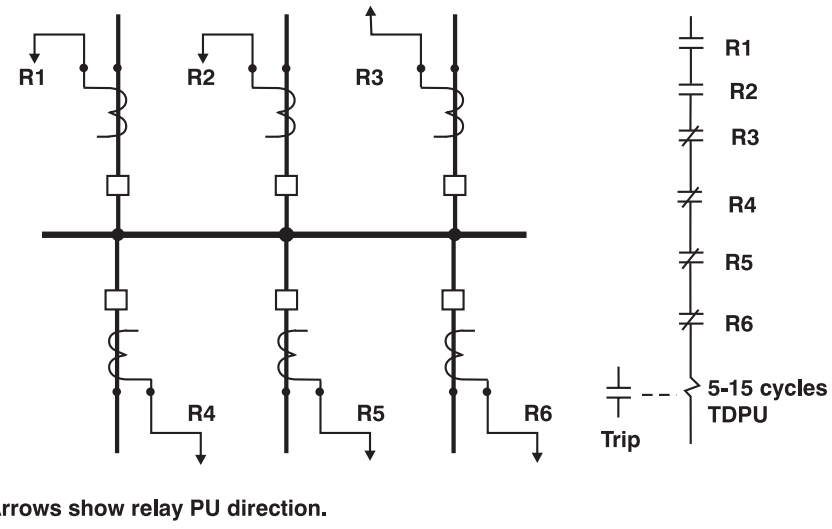

Figure 25: Transmission Interlocked Bus Protection Schematic, Dependable Scheme

For additional security the logic can be set up so that more than one relay looking into the bus must see the fault. But the net security of this scheme is directly dependent on the net reliability of each of the blocking elements in the scheme. This is a system requiring very high line relay reliability. Since this scheme must be blocked by relays that look outward from the bus, it requires a coordinating time delay similar to that used in the radial substation logic. The time delay needs to be longer than the slowest blocking element. The time delay requirements may cause a race with remote line relay Zone 2 tripping elements.

TIME OVERCURRENT RELAYING

Basic Concept

Time overcurrent relaying is, of course, a relatively slow way to clear a bus fault, but it is ideal and inexpensive for the multitude of small substations with buses that can handle the available fault current for a short time.

Bus Main And Tie OC Relays

The approach is fairly straightforward and the concept does not need much development. Basically, an overcurrent relay is placed on the bus (and bus tie, if it exists) to coordinate with the feeder breakers and transformer overcurrent relays and/or transformer damage curves (IEEE C37.91). The pickup of the phase elements of the bus main and bus tie relays may be chosen for bus overload protection. Typical overcurrent relaying coordination curves are shown in fig. 26. Fig. 26 is the coordination curve for a system approximately like Fig. 27, with one bus source. However, if the bus main and bus tie may be closed simultaneously, the coordination slows. For instance, the bus main may be set to pick up at 3000A. For a 10,000A fault, it either sees 10000A if it is the only source, or maybe 5000A if the tie is closed. Pickup coordination becomes very difficult unless some adaptive approach to relay pickup is used, employing a digital intelligent relay that monitors system conditions.

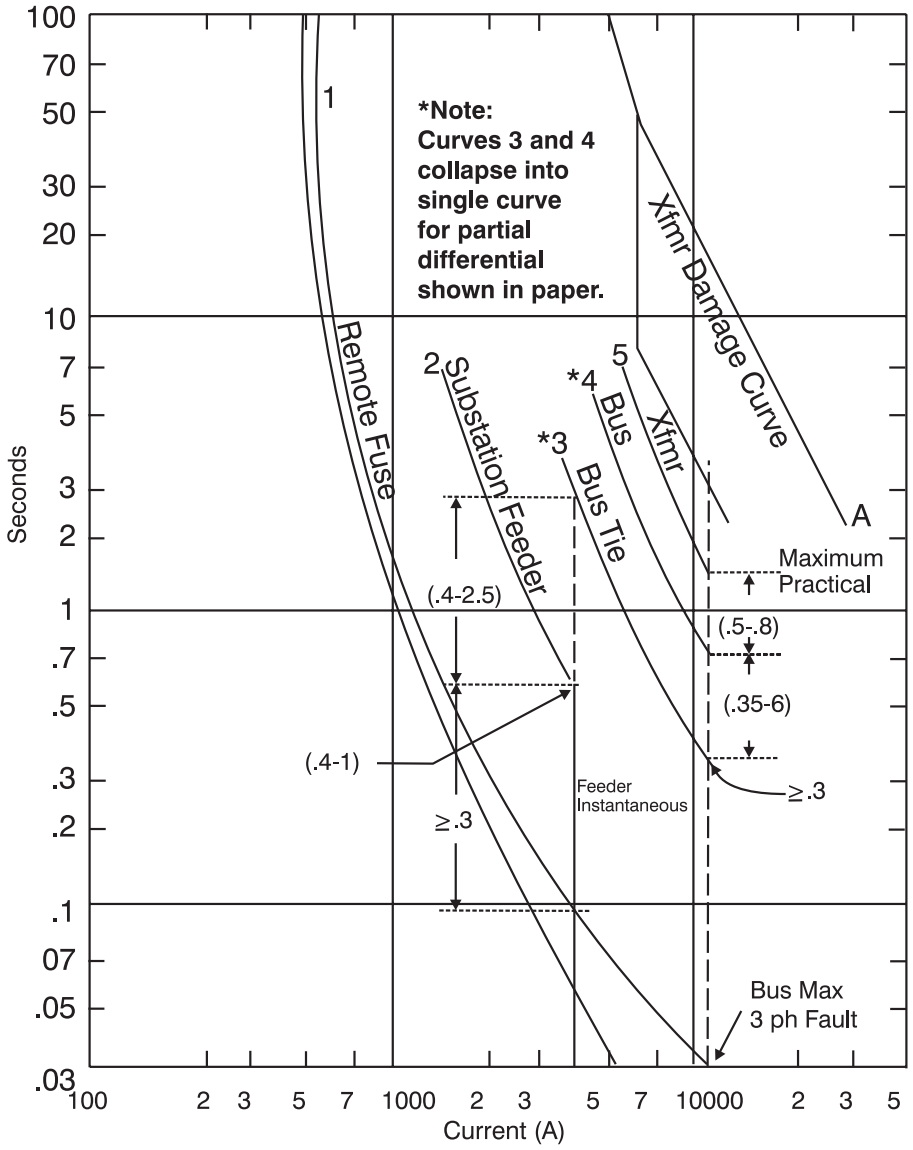

Figure 26: Typical Distribution Bus Phase Overcurrent Protection, Partial Differential

Partial Differential

The partial differential relay is an overcurrent relay that monitors a summation of a subset of the sources and/or loads of a substation. There is no set approach to which CTs would be included in the summation, but two variations that show the range are 1) a scheme that sums just the sources into a bus (see fig. 27), and 2) a scheme that sums all but one or several feeder currents when the tie is closed (as might happen if one or more feeders are fused bus taps without CTs).

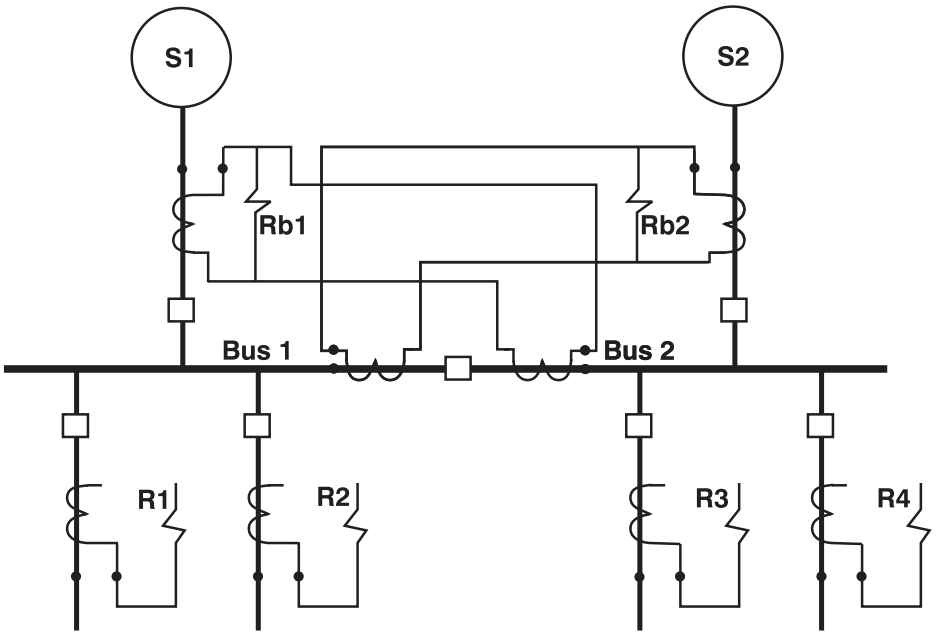

Figure 27: Partial Differential, Summation of Main and Tie

In the scheme, an overcurrent relay is connected to the partial differential summation. The overcurrent relay must coordinate with the remaining overcurrent relays on the bus that are not part of the differential scheme. By summing the bus tie and bus main, the number of overcurrent elements in the coordination study is reduced by one, which can be helpful when the coordination curves are tight. The scheme simplifies the overcurrent pickup shift problem associated with multiple sources into a bus. Similar to the interlocked relay design, the partial differential element can have a high speed trip output with a small delay that is blocked if any remaining feeder sees an overcurrent condition.

OTHER SCHEMES

Other approaches to bus protection that are relatively less commonly used, at least in the U.S., but may be common at certain utilities, are:

Linear Coupler Relaying

Linear coupler relaying uses special air core CTs. Because air core CTs have minimal burden capabilities, the CTs may be considered voltage sources rather than current sources. They produce a voltage proportionate to line current. The practice is to connect all CTs feeding a bus in series. If the voltages sum to zero, then current in equals current out. If there is a net voltage, then a bus fault has occurred.

Isolated Ground Bus Fault Detection

In some bus designs where virtually all faults will involve ground, such as in metal clad switchgear, it is possible to monitor for a bus fault by only monitoring ground current. The application to metal clad switchgear is easiest to understand conceptually. The pro-

cess requires the entire frame of the switchgear to be isolated from ground, except a single connection that is monitored via an overcurrent relay. This isolation could possibly be a more expensive effort than putting in dedicated relaying. If there is a phase to switchgear frame fault, the current flows from the frame to ground via the single connection to ground, and the fault is detected and the bus tripped.

Ground Differential

A condition where ground differential has been used is when there are no CTs that can be dedicated toward a bus differential circuit. A bus ground differential is a possible alternate protection scheme. The CTs on all three phases on every line leaving the bus can be directed to the appropriate line relay or transformer relay, then summed to create the bus ground current, and finally fed into a differential or overcurrent relay. Either a high impedance or low impedance relay will work.

DEPENDABILITY AND SECURITY ISSUES

Dependability: Backup Tripping

One difficulty with bus protection is that there is frequently no local backup protection. If the bus protection fails, the remote line relays are expected to sense the fault and clear the substation. This typically will occur in the line relay delays associated with zone 2 or even zone 3 relaying, or typically 20-40 cycles. This, of course, will make a bad situation worse. Remote relay sensitivity is not usually an issue, but may be. The concern is that the source of the problem takes longer to identify, more of the system is lost than is required, it is likely worse for systems stability, and the system and load restoration takes much longer.

There is no backup protection because a bus protection system typically requires dedicated CTs. However, the dependability of the typical bus differential system is high, so lack of dedicated backup tripping is typically accepted.

One possible backup protection method is the interlocked line relaying design. This type of design uses existing relays and can be set up to operate faster than zone 2 line relays.

In the typical case, if backup bus protection exists, there is some desire for it to be faster than the remote line relaying and possibly faster than the breaker failure relay. The breaker failure relay may become involved if the bus relay tripped but the trip did not reach the breakers. Hence, depending on what the backup relaying is coordinating with, it typically must be faster than 20 cycles, or even 10 cycles if breaker failure relaying is involved.

Security: Fault Verification Before Tripping

The magnitude of the effects of a bus relay operation leads to concerns about relay security. Bus protection relaying tends to be fairly sensitive. If backup protection is added, there is even less security. However, security in a bus differential relay might imply adding a supervisory relay that will block a bus relay when the supervisory relay does not sense a

fault. If this occurs, and even if the condition is due to some operator error and no fault exists, it is possibly unsafe to block the relay from tripping. The current and voltage levels involved in the CT secondary circuit may be high and the relay could quickly be destroyed, nearby equipment could be damaged, and personnel could be hurt.

If one can justify the design effort and risk, a way to add at least a certain amount of security is to have a fault detector separate from any fault detector in the relay supervise the operation of the bus relay. One difficult part of the scheme is ensuring that the fault detector setup sees a bus fault for any possible bus configuration. The relay chosen must operate quickly. It should operate as fast or faster than the bus differential relay, and it must sense the misoperation of the bus relay and remove it from service before it is damaged, while not tripping the bus, which adds to a difficult demand.

References

[1] IEEE C37.97 (Reaffirmed 12/90), IEEE Guide for Protective Relay Applications to Power System Buses

[2] Blackburn, J. Lewis, Protective Relaying, Principles and Applications,2nd Edition, New York: Marcel Dekker, 1998

[3] Elmore, Walter A., ed., ABB Inc. Protective Relaying, Theory and Applications, New York: ABB/Marcel Dekker, 1994

[4] Protective Relay Application Guide, Third Edition, London: GEC Alsthom T&D/ Balding & Mansell, 1987

[5] IEEE C37.110 (1996), IEEE Guide for the Application of Current Transformers Used for Protective Relay Purposes

[6] Wentz E.C., Sonneman, W.K., “Current Transformers and Relays for High Speed Differential Protection, With Particular Reference to Offset Transient Currents,” *AIEE Transactions, Part III, vol. 59, pp481-488, 1940*. Reprinted in Stanley H. Horowitz, editor, “Protective Relaying for Power Systems,” IEEE Press, 1980, a volume of selected power engineering reprints under sponsorship of IEEE PES.

[7] Conner, E.E., Wentz, E.C., Allen, D.W., “Methods For Estimating Transient Performance of Practical Current Transformers for Relaying,” *IEEE Trans. Power Apparatus Systems,* PAS 94, Jan. 1975, pp 116-122.

[8] Hodgkiss, J.W., "The Behaviour of Current Transformers Subjected to Transient Asymmetric Currents and the Effects on Associated Protective Relays," CIGRE Paper Number 329, Session 15-25, June 1960

[9] "Transient Response of Current Transformers," Power System Relaying Committee Report 76-CH1130-4 PWR, IEEE Special Publication, 1976

[10] Allan Greenwood, Electrical Transients in Power Systems, Second Edition, John Wiley & Sons, 1991

[11] "Bus Differential Protection - Application of PVD Relays Using Different Ratio Current Transformers," General Electric Publication GER-6455, available on GE CD ROM Catalog and GE Web Site

[12] Instruction Manual, Static Differential Relay For Bus Protection, SBD11B, General Electric Publication GEK-45451C

[13] Instruction Manual, Differential Voltage Relays, PVD21A, PVD21B, PVD21C, PVD21D, General Electric Publication GEK-45405D

[14] Instruction Manual, Single Phase and Three Phase Bus Differential Relays, Model BE1-87B, Basler Electric Publication Number 9282300990.

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This paper has evolved and has been updated by John Horak since original 1998 publication.

APPENDIX A: BUS DESIGN

TYPICAL BUS ARRANGEMENTS

The bus arrangements evaluated in this paper are:

- Single breaker - single bus
- Double bus with bus tie
- Double bus - single breaker
- Double bus - double breaker
- Ring bus
- Breaker-and-a-half bus
- Main and transfer bus
- No bus - The Tapped Line

Single breaker - Single bus

This is the most basic and simple bus arrangement. The bus readily can be protected by a bus differential relay utilizing line-side CTs on all breakers. It is an economical installation utilizing a minimum number of breakers and no breaker bypass facilities. Maintenance on breaker or relays requires the removal of the line associated with the breaker. Single breaker/single bus arrangements are primarily used to service industrial applications where lines 1 and 2 terminate at a remote bus and lines 3 and 4 terminate at a remote bus. Thus, the removal of line 1 would not disrupt service to the remote bus supplied by lines 1 and 2. Provisions must be made to ensure that each line can adequately carry the total load.

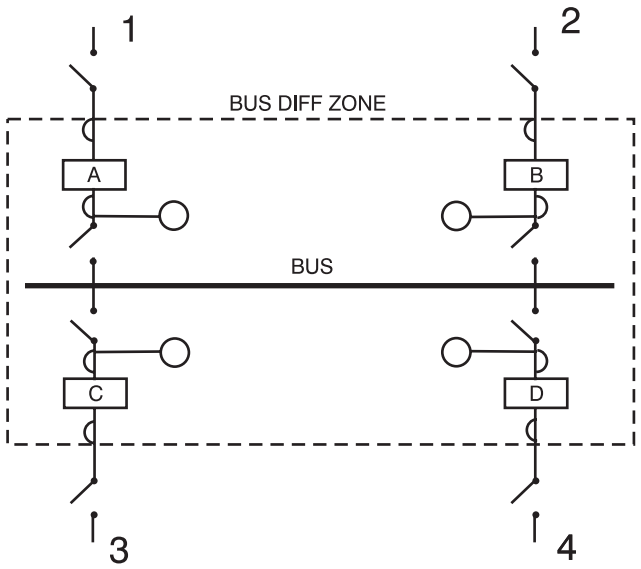

Figure B1: Single Breaker, single bus

Double bus with bus tie

This bus arrangement is a logical extension of the single breaker/single bus concept with provisions to isolate two bus sections. The installation of a bus tie breaker T creates two bus sections, A and B. Under these conditions a bus fault will de-energize two line sections while retaining service to the remaining two line sections. This type of installation is used where two lines terminate at one bus. For example, line 1 and line 3 would terminate at a common bus and line 2 and line 4 would terminate at a common bus. Thus, the loss of either bus section would not interrupt service to the remote bus terminals. However, a circuit must be removed for breaker or relay maintenance and a failure in breaker T will de-energize the entire station.

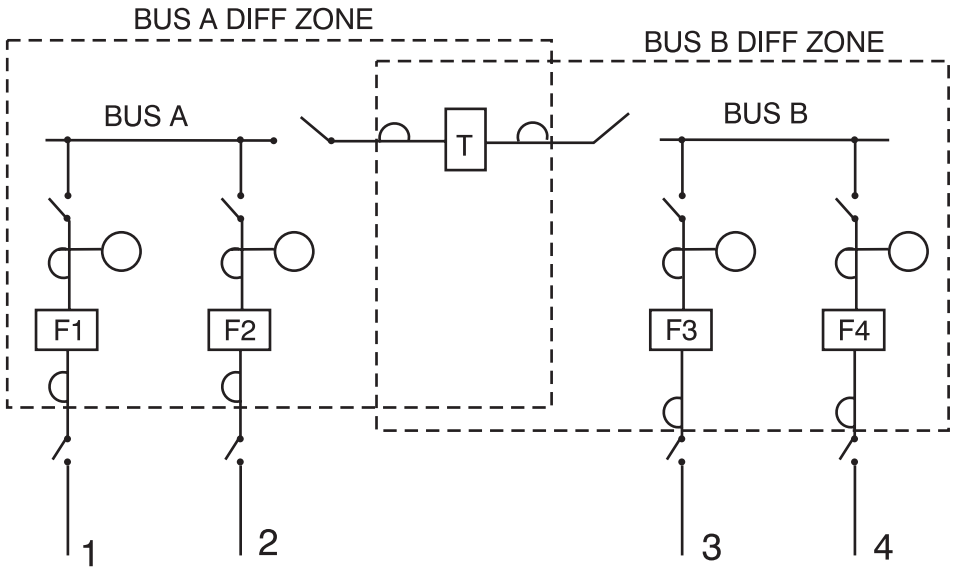

Figure B2: Double bus with bus tie

Double bus - Single breaker

Fig. B3 depicts the normal setup of a double bus/single breaker scheme. Breakers F1 and F2 are served from bus 1 and employ a bus differential arrangement from the line-side CTs of the feeder breakers and the bus 2 side CTs of breaker T. A similar bus differential arrangement is employed around breakers F3, F4, and T. This bus arrangement differs from the double bus with bus tie because it utilizes the tie breaker as a spare breaker when maintenance is to be done on any feeder breaker. A bus fault will de-energize two circuits. Therefore, this scheme is usually used where two lines (example - F1 and F3) terminate to a common bus. F2 and F4 would also terminate on a common bus.

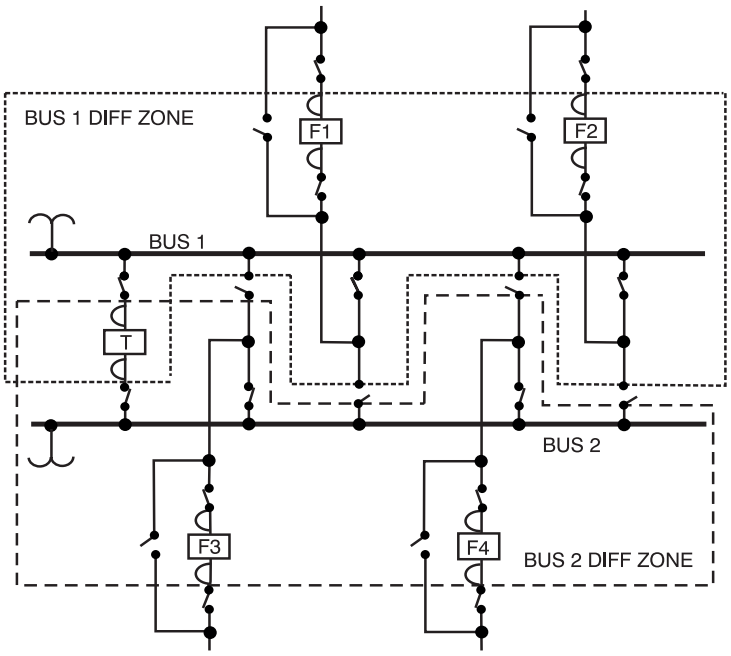

Figure B3: Double bus, single breaker (Normal)

Fig. B4 depicts breaker F1 off line and out for maintenance. Breaker T can be utilized as a spare breaker where bus 1 becomes an extension of line 1. To accomplish this, F2 must be transferred to bus 2 and the differential scheme for bus 2 must accommodate breaker F2. It is illustrated that the switching arrangements can be complicated and subject to misoperation. Under normal conditions a fault in the tie breaker T will result in a complete station outage.

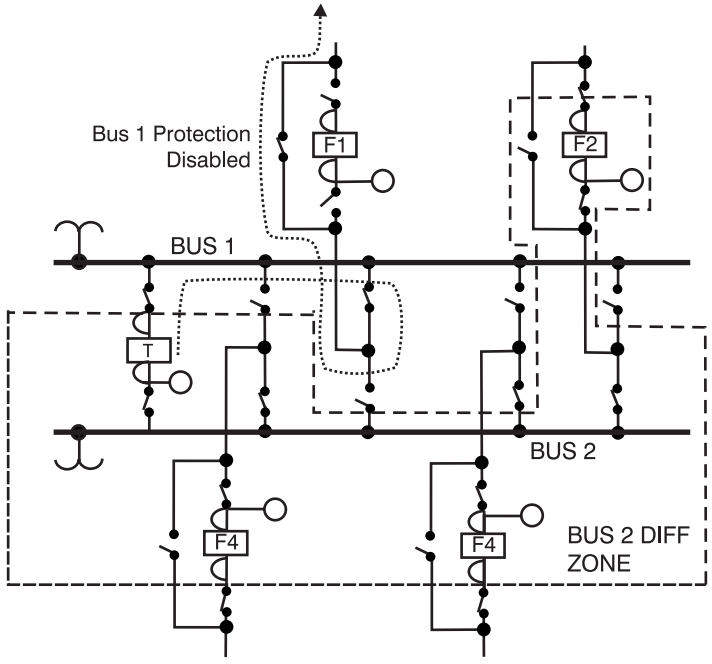

Figure B4: Double bus, single breaker (F1 off line)

Double bus - Double breaker

This arrangement has high flexibility. Either bus can be removed from service without de-energizing any lines. A disadvantage of this bus arrangement is that it takes two breakers to clear a line fault, thus doubling the opportunity for a breaker failure. During breaker maintenance, relays have to remain in service on the adjoining breaker to provide line protection. Line-side PTs are required which may adversely affect impedance relay performance for line faults where voltage restraint goes to zero when the line is de-energized. However, impedance relays are built to accommodate line-side potentials by the inclusion of overcurrent relays that monitor the trip circuit. However, these overcurrent relays must be set low enough to detect remote-end faults to ensure correct operation.

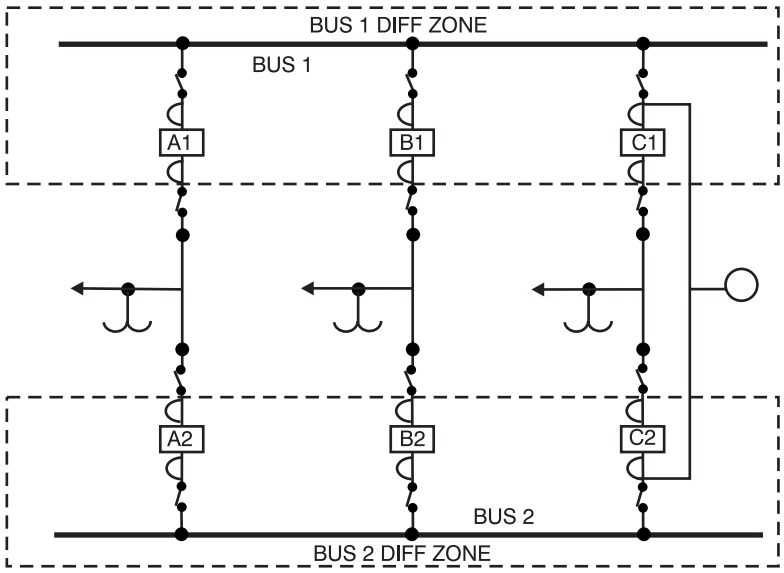

Figure B5: Double bus, double breaker

Ring Bus

The ring bus is commonly used at higher voltages because it is economical, requiring the minimum number of breaker for the number of lines served. It also has high flexibility in that breakers can be removed from service for maintenance with a minimum amount of switching. A switch is needed at the line exit so that the line can be isolated without leaving the ring broken.

A ring bus is not without its disadvantages. With a breaker out for maintenance, a subsequent fault will split the ring. For example, in fig. B6, if breaker E is out of service for maintenance and a fault occurs on line 4, lines 3 and 5 will be isolated from lines 1 and 2. Therefore, whenever a ring is established, design engineers must evaluate a variety of operating scenarios to ensure that isolated line segments will not adversely affect the system. As in other bus arrangements during breaker maintenance, relays must remain in service and line-side PTs must be utilized to provide restraint for impedance relays. All faults also must trip two breakers, thereby increasing the probability of a breaker failure.

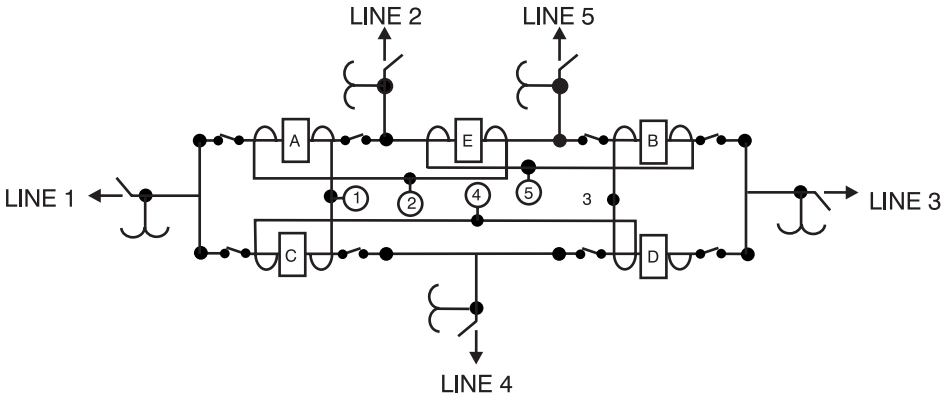

Figure B6: Ring bus - 5 point

Breaker-and-a-half

Breaker-and-a-half schemes are commonly used because they provide good operating flexibility. They require more breakers than a ring bus to serve the same number of lines.

They also use line-side potentials, and two breakers must operate for every line fault. A bus differential will not cause any line interruptions. Also, two lines can be interrupted for breaker maintenance on one line. For example, in fig. B7 a breaker outage on B2 and a subsequent fault on line 2 will de-energize both line 2 and line 3.

In fig. B7, the location of bank 2 in relation to bank 1 is important to ensure that both banks are not de-energized for a common failure mode. For example, if bank 2 were located in the line 1 position, the common failure mode would be breaker TA which would cause both banks to be de-energized. Again, a design engineer must evaluate all failure mode scenarios to ensure that operating constraints are kept to a minimum.

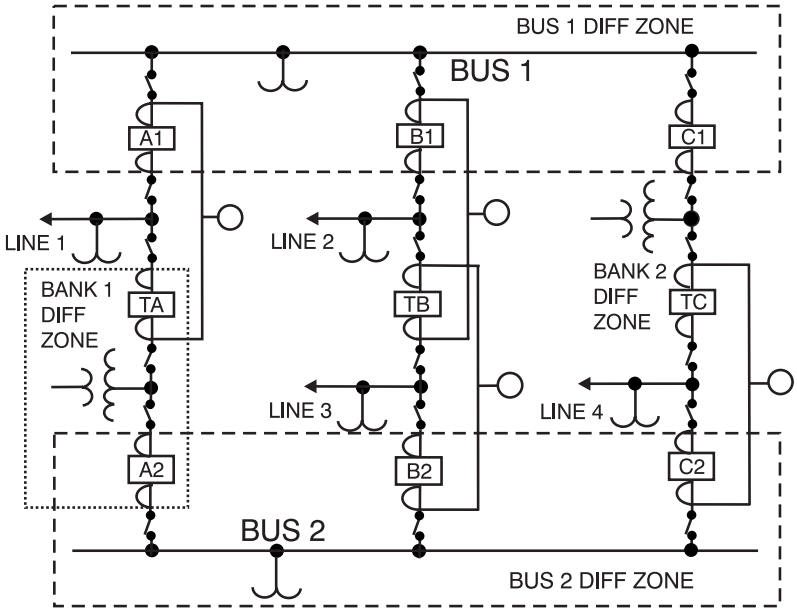

Figure B7: Breaker-and-a-half

Main and transfer bus

A three-line substation with a main and transfer bus arrangement is shown in Fig. B8. Under normal conditions the three lines are connected through breakers 1, 2, and 3 to a main bus. When breaker 1, 2, or 3 is removed from service, load is transferred to the transfer bus and relaying for breaker T is set appropriately.

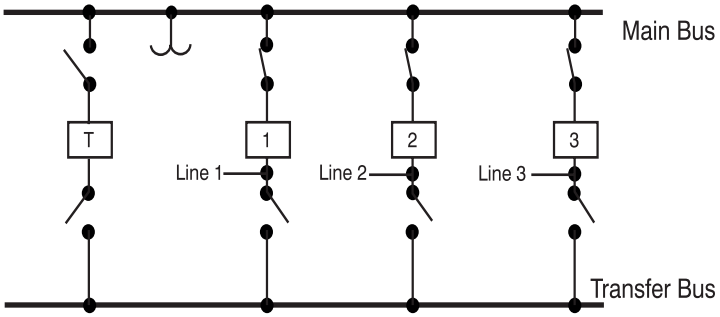

Figure B8: Main and Transfer Bus

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